CY7C371i

UltraLogic™ 32-Macrocell Flash CPLD

Features

- **32 macrocells in two logic blocks**
- **32 I/O pins**
- **5 dedicated inputs including 2 clock pins**
- **In-System Reprogrammable (ISR™) Flash technology**
  - **JTAG interface**
- **Bus Hold capabilities on all I/Os and dedicated inputs**
- **No hidden delays**
- **High speed**
  - **f_{MAX} = 143 MHz**
  - **t_{PD}= 8.5 ns**
  - **t_S = 5 ns**
  - **t_{CO} = 6 ns**
- **Fully PCI compliant**
- **3.3V or 5.0V I/O operation**
- **Available in 44-pin PLCC, and TQFP packages**
- **Pin compatible with the CY7C372i**

Functional Description

The CY7C371i is an In-System Reprogrammable Complex Programmable Logic Device (CPLD) and is part of the FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C371i is designed to bring the ease of use and high performance of the 22V10, as well as PCI Local Bus Specification support, to high-density CPLDs.

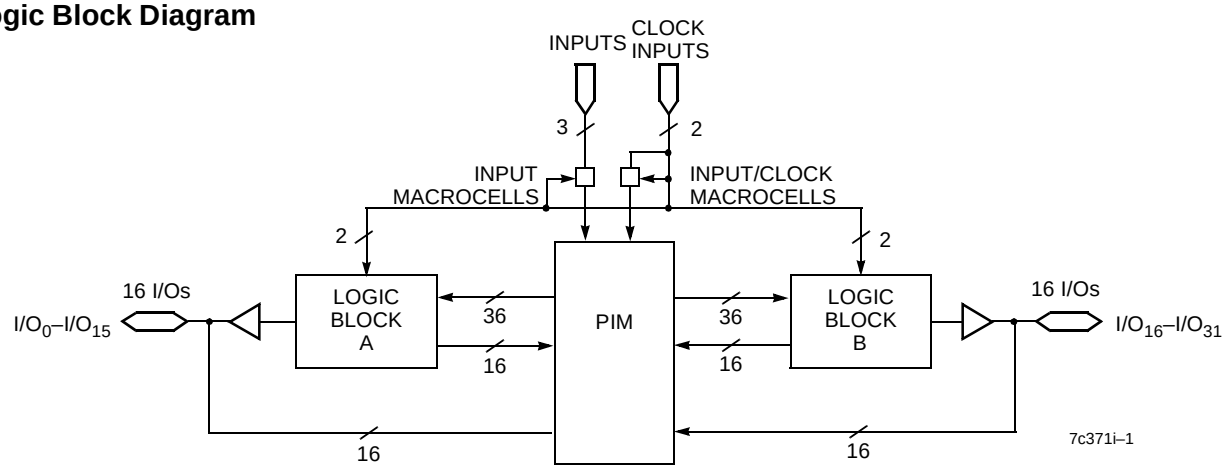
Like all of the UltraLogic™ FLASH370i devices, the CY7C371i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The Cypress ISR function is implemented through a JTAG serial interface. Data is shifted in and out through the SDI and SDO pins. The ISR interface is enabled using the programming voltage pin (ISR_{EN}). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 32 macrocells in the CY7C371i are divided between two logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370i family, the CY7C371i is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY7C371i. In addition, there are three dedicated inputs and two input/clock pins.

Logic Block Diagram



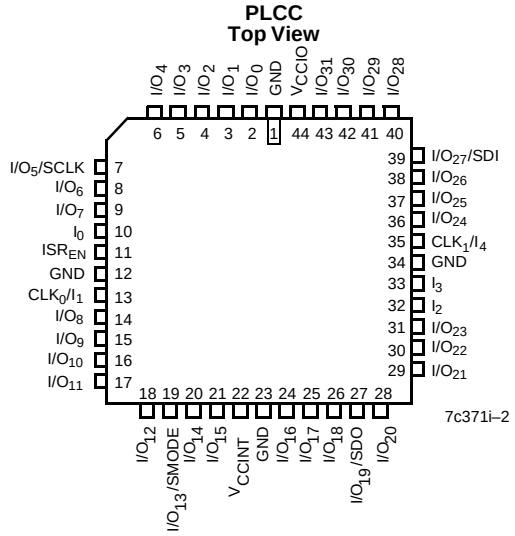
Selection Guide

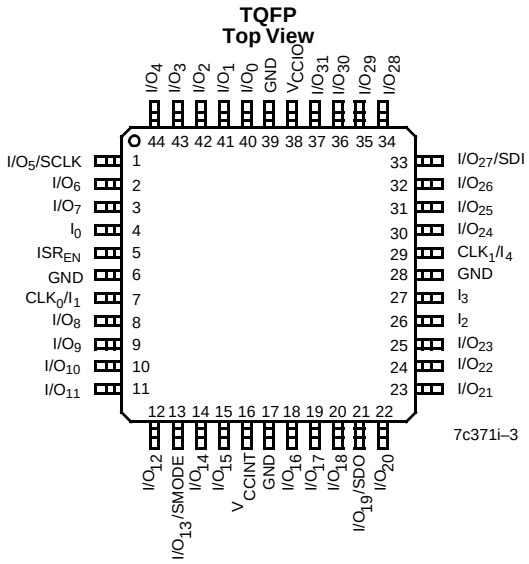
		7C371i-143	7C371i-110	7C371i-83	7C371iL-83	7C371i-66	7C371iL-66
Maximum Propagation Delay[1], t_{PD} (ns)		8.5	10	12	12	15	15
Minimum Set-Up, t_S (ns)		5	6	8	8	10	10
Maximum Clock to Output[1], t_{CO} (ns)		6	6.5	8	8	10	10
Typical Supply Current, I_{CC} (mA)	Comm./Ind.	75	75	75	45	75	45

Note:

1. The 3.3V I/O mode timing adder, $t_{3.3IO}$, must be added to this specification when V_{CCIO} = 3.3V.

Pin Configurations





Functional Description (continued)

Finally, the CY7C371i features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C371i remain the same.

Logic Block

The number of logic blocks distinguishes the members of the FLASH370i family. The CY7C371i includes two logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370i logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in a single pass through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370i CPLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C371i has a separate associated I/O pin. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed. It also has polarity control, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the two logic blocks on the CY7C371i to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Programming

For an overview of ISR programming, refer to the FLASH370i Family data sheet and for ISR cable and software specifications, refer to ISR data sheets. For a detailed description of ISR capabilities, refer to the Cypress application note, “An Introduction to In System Reprogramming with FLASH370i.”

PCI Compliance

The FLASH370i family of CMOS CPLDs are fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The simple and predictable timing model of FLASH370i ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without simple and predictable timing, PCI compliance is dependent upon routing and product term distribution.

3.3V or 5.0V I/O operation

The FLASH370i family can be configured to operate in both 3.3V and 5.0V systems. All devices have two sets of V_{CC} pins: one

set, VCCINT, for internal operation and input buffers, and another set, VCCIO, for I/O output drivers. VCCINT pins must always be connected to a 5.0V power supply. However, the VCCIO pins may be connected to either a 3.3V or 5.0V power supply, depending on the output requirements. When VCCIO pins are connected to a 5.0V source, the I/O voltage levels are compatible with 5.0V systems. When VCCIO pins are connected to a 3.3V source, the input voltage levels are compatible with both 5.0V and 3.3V systems, while the output voltage levels are compatible with 3.3V systems. There will be an additional timing delay on all output buffers when operating in 3.3V I/O mode. The added flexibility of 3.3V I/O capability is available in commercial and industrial temperature ranges.

Bus Hold Capabilities on all I/Os and Dedicated Inputs

In addition to ISR capability, a new feature called bus-hold has been added to all FLASH370i I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Design Tools

Development software for the CY7C371i is available from Cypress's *Warp*™, *Warp* Professional™, and *Warp* Enterprise™ software packages. Please refer to the data sheets on these products for more details. Cypress also actively supports almost all third-party design tools. Please refer to third-party tool support for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs (LOW)..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC} V_{CCINT}	V_{CCIO}
Commercial	0°C to +70°C	5V ± 0.25V	5V ± 0.25V OR 3.3V ± 0.3V
Industrial	–40°C to +85°C	5V ± 0.5V	5V ± 0.5V OR 3.3V ± 0.3V

Electrical Characteristics Over the Operating Range[2,3]

Param.	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage with Output Enabled	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[8]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l/Ind)[4,5]			4.0	V
			I_{OH} = –50 µA (Com'l/Ind)[4,5]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs[6]		2.0		7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs[6]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = Internal GND, V_I = V_{CC}		–10		+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_O = GND or V_O = V_{CC}, Output Disabled		–50		+50	µA
		V_{CC} = Max., V_O = 3.3V, Output Disabled[5]		0	–70	–125	µA
I_{OS}	Output Short Circuit Current[7,8]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = 1 MHz, V_{IN} = GND, V_{CC}[9]	Com'l/Ind.		75	125	mA
			Com'l "L" –66, –83		45	75	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Capacitance[8]

Parameter	Description	Test Conditions	Min.	Max.	Unit
$C_{I/O}$[10]	Input Capacitance	V_{IN} = 5.0V at f=1 MHz		8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz	5	12	pF

Inductance[8]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f= 1 MHz	2	5	nH

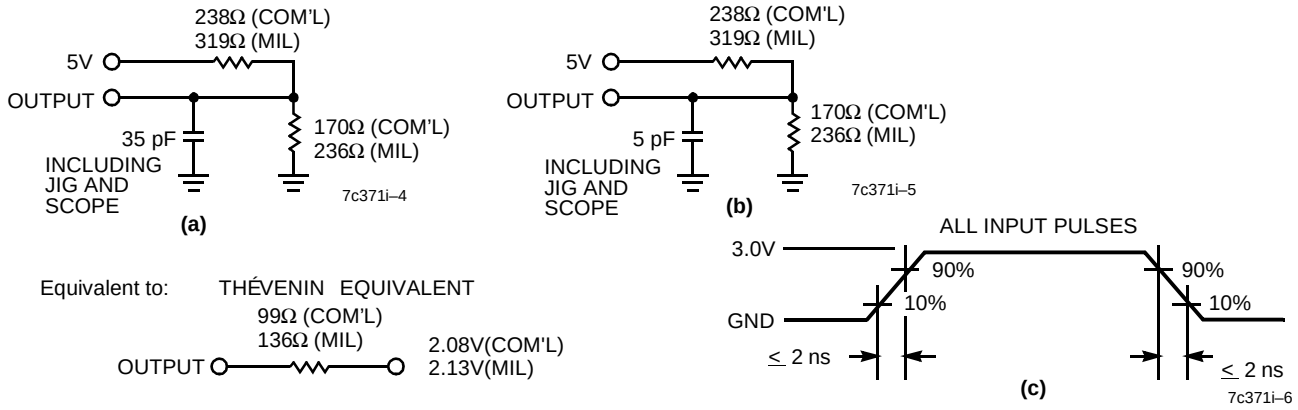
Endurance Characteristics[8]

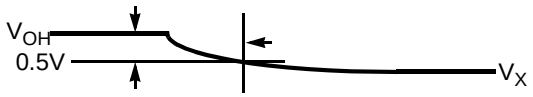
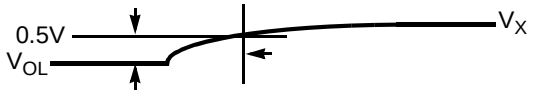
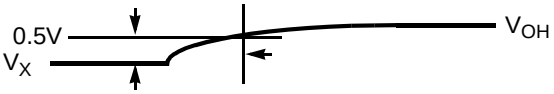
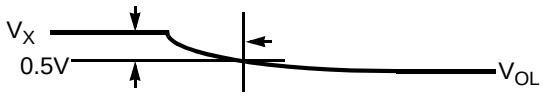
Parameter	Description	Test Conditions	Max.	Unit
N	Maximum Reprogramming Cycles	Normal Programming Conditions	100	Cycles

Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. If V_{CCIO} is not specified, the device can be operating in either 3.3V or 5V I/O mode; V_{CC}=V_{CCINT}.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for SDO.
5. When the I/O is three-stated, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are three-stated during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
6. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
7. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
8. Tested initially and after any design or process changes that may affect these parameters.
9. Measured with 16-bit counter programmed into each logic block.

AC Test Loads and Waveforms



Parameter[11]	Vx	Output Waveform Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

Notes:
10. CI/O for ISR_{EN} is 15 pF Max.
11. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	7C371i–143		7C371i–110		7C371i–83 7C371iL–83		7C371i–66 7C371iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output[1]		8.5		10		12		15	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch[1]		11.5		13		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches[1]		13.5		15		20		24	ns
t_{EA}	Input to Output Enable[1]		13		14		19		24	ns
t_{ER}	Input to Output Disable		13		14		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[8]	2.5		3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	2.5		3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output[1]		12		14		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch[1]		14		16		21		26	ns
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output[1]		6		6.5		8		10	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	5		6		8		10		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)[1]		12		14		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	7		9		12		15		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	9		10		12		15		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[8]	143		111		83.3		66.6		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[8]	166.7		153.8		100		83.3		MHz
f_{MAX3}	Maximum Frequency with external feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)[8]	91		80		50		41.6		MHz
t_{OH}-t_{IH} 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[8,13]	0		0		0		0		ns

Notes:

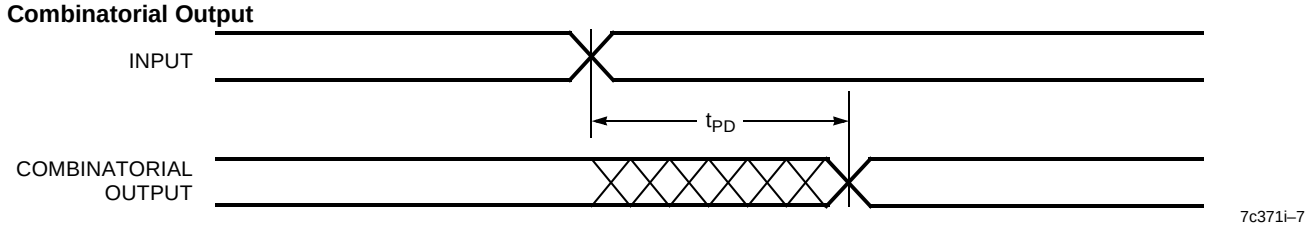
12. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
13. This specification is intended to guarantee interface compatibility of the other members of the CY7C370i family with the CY7C371i. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

Switching Characteristics Over the Operating Range[12] (continued)

Parameter	Description	7C371i–143		7C371i–110		7C371i–83 7C371iL–83		7C371i–66 7C371iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	7		9		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	125		111		76.9		62.5		MHz
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[8]	8		10		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[8]	10		12		17		22		ns
t_{RO}	Asynchronous Reset to Output[1]		14		16		21		26	ns
t_{PW}	Asynchronous Preset Width[8]	8		10		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[8]	10		12		17		22		ns
t_{PO}	Asynchronous Preset to Output[1]		14		16		21		26	ns
Tap Controller Parameters										
f_{TAP}	Tap Controller Frequency	500		500		500		500		kHz
3.3V I/O Mode Parameters										
$t_{3.3IO}$	3.3V I/O mode timing adder		1		1		1		1	ns

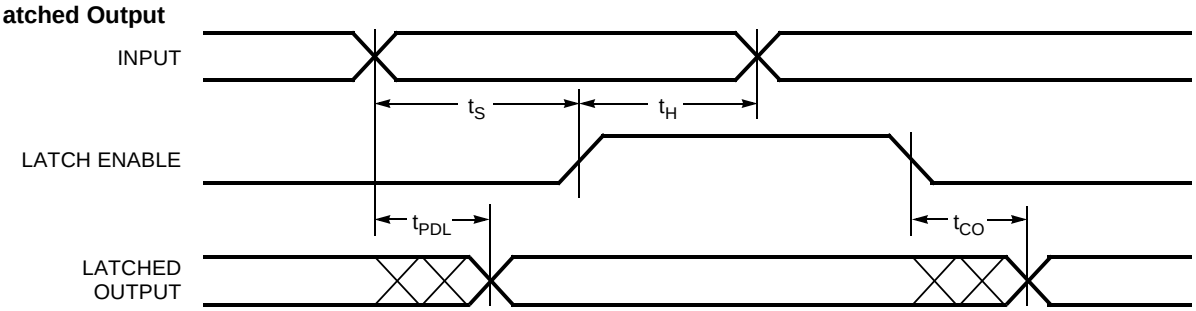
Switching Waveforms

Combinatorial Output



7c371i–7

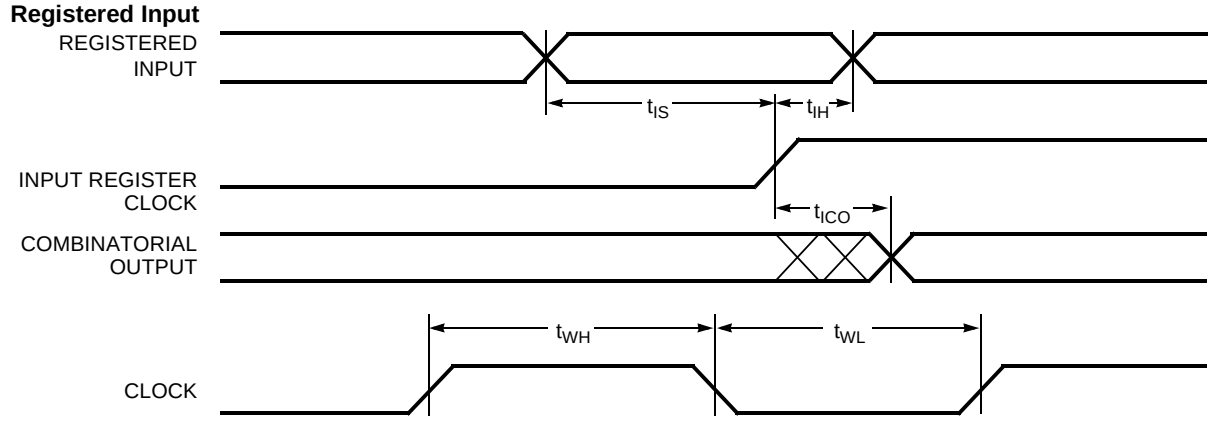
atched Output



7c371i–8

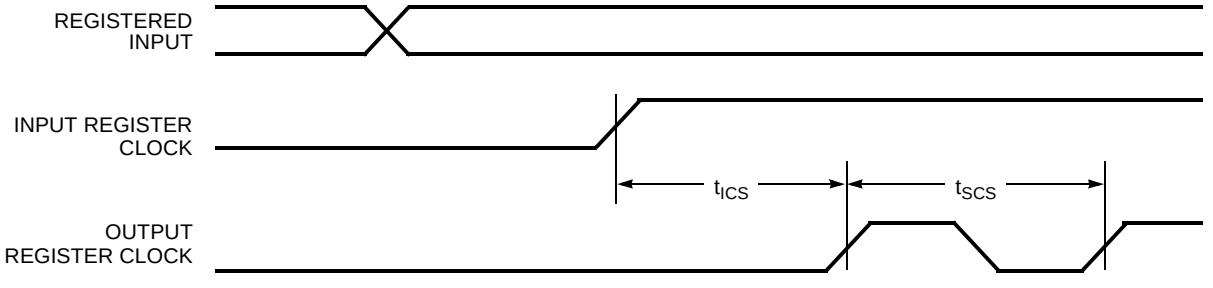
Switching Waveforms (continued)

Registered Input



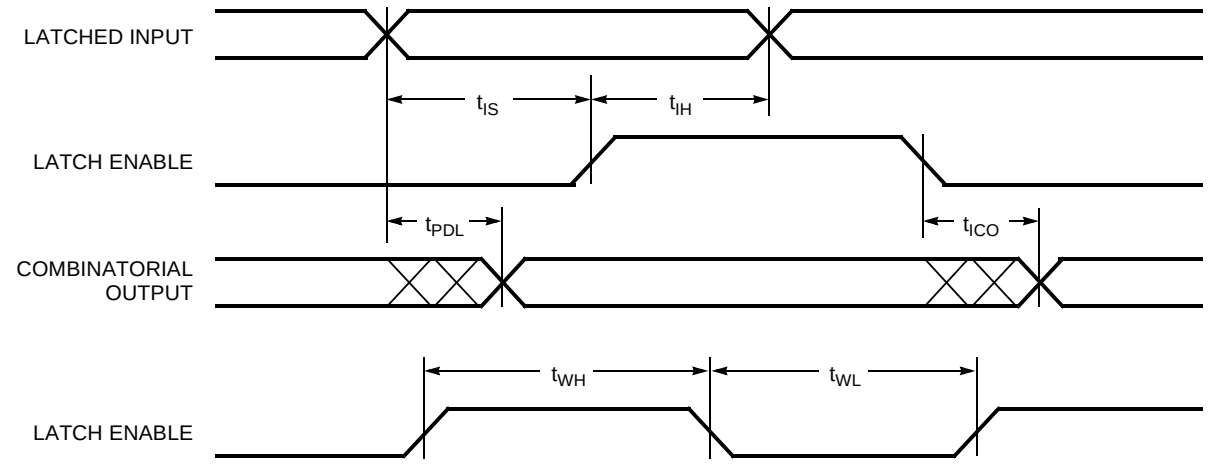
7c371i–9

Clock to Clock



7c371i–10

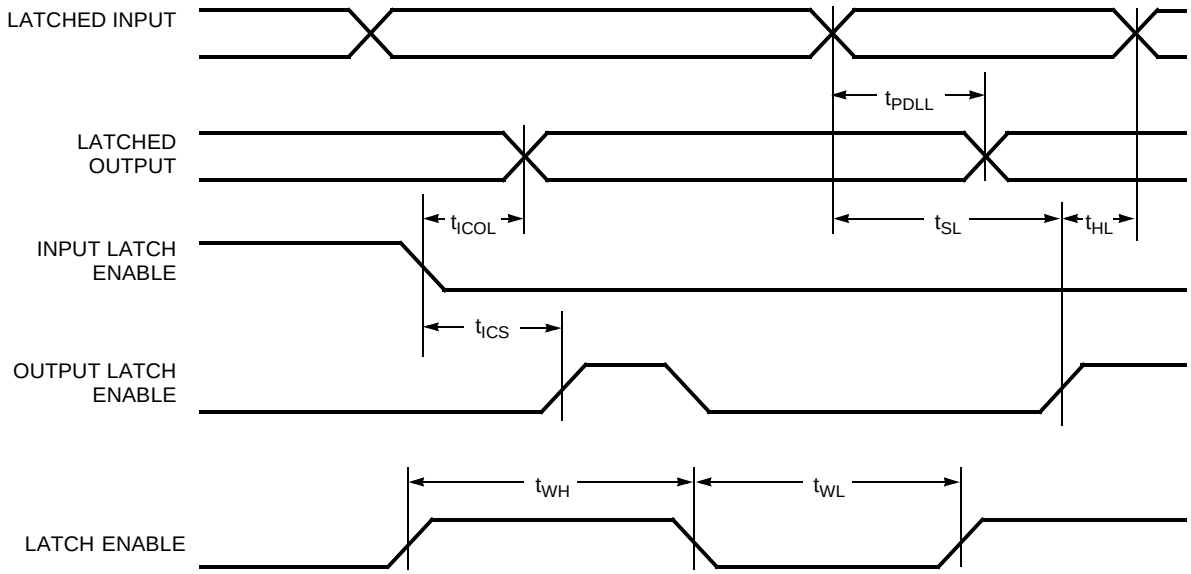
Latched Input



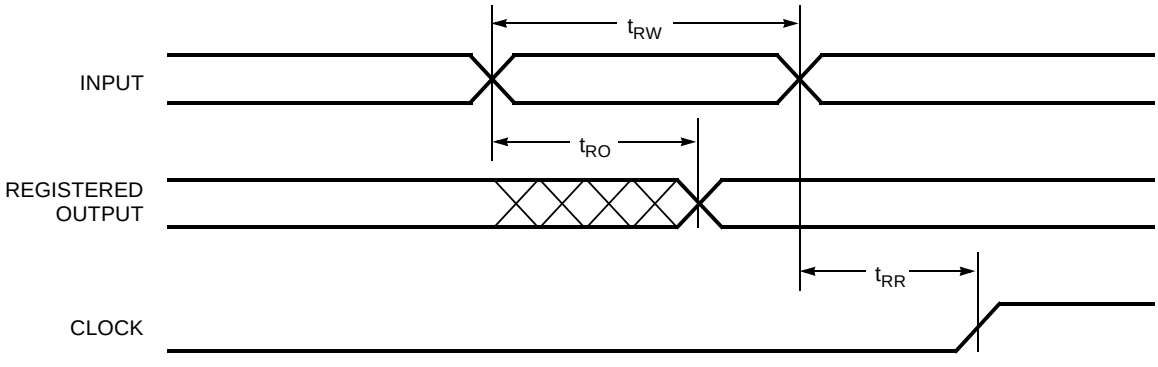
7c371i–11

Switching Waveforms (continued)

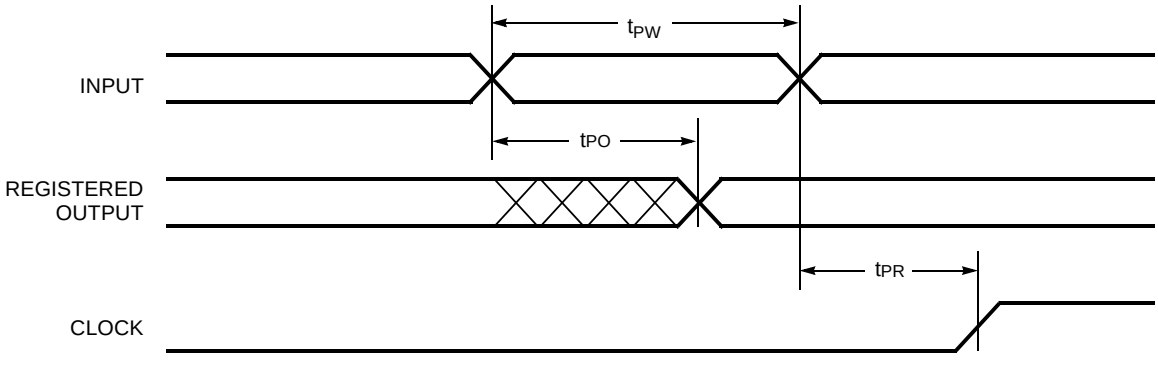
Latched Input and Output



Asynchronous Reset

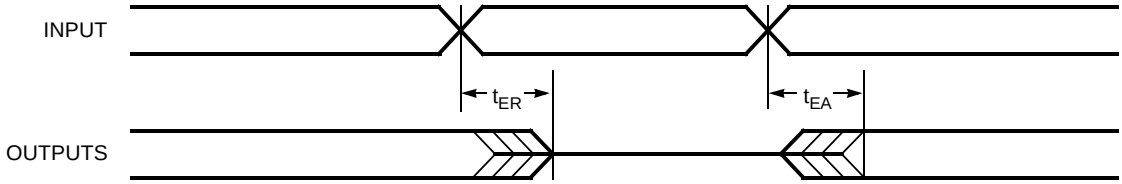


Asynchronous Preset



Switching Waveforms (continued)

Output Enable/Disable



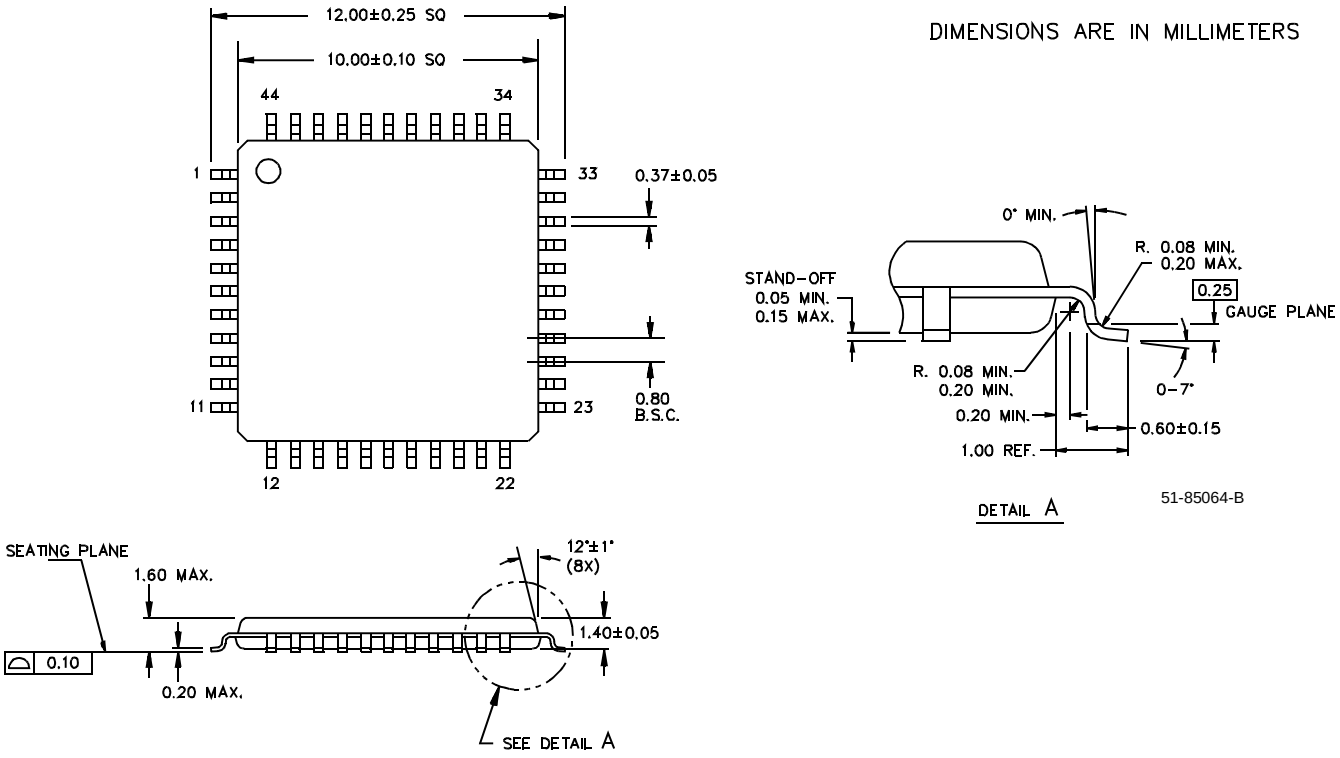
7c371i–16

Ordering Information

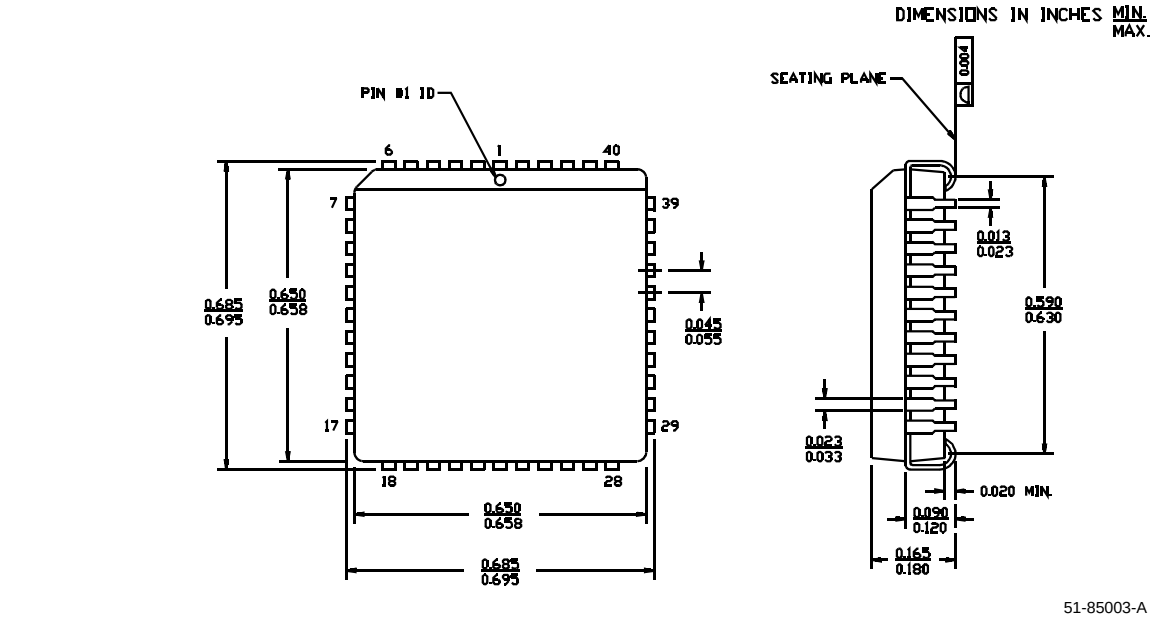
Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
143	CY7C371i–143AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i–143JC	J67	44-Lead Plastic Leaded Chip Carrier	
110	CY7C371i–110AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i–110JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371i–110AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371i–110JI	J67	44-Lead Plastic Leaded Chip Carrier	
83	CY7C371i–83AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i–83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371i–83AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371i–83JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL–83AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371iL–83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL–83AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371iL–83JI	J67	44-Lead Plastic Leaded Chip Carrier	
66	CY7C371i–66AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i–66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371i–66AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371i–66JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL–66AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371iL–66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL–66AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371iL–66JI	J67	44-Lead Plastic Leaded Chip Carrier	

Package Diagrams

44-Lead Thin Plastic Quad Flat Pack A44



44-Lead Plastic Leaded Chip Carrier J67



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**	106377	06/18/01	SZV	Change from Spec #: 38-00497 to 38-03032