



	PLA110L	Units
Load Voltage	400	V
Load Current	150	mA
Max R_{ON}	25	Ω

Features

- Small 6 Pin DIP Package
- Low Drive Power Requirements (TTL/CMOS Compatible)
- No Moving Parts
- High Reliability
- Arc-Free With No Snubbing Circuits
- 3750V_{RMS} Input/Output Isolation
- No EMI/RFI Generation
- Machine Insertable, Wave Solderable
- Current Limiting, Surface Mount and Tape & Reel Versions Available

Applications

- Telecommunications
 - Telecom Switching
 - Tip/Ring Circuits
 - Modem Switching (Laptop, Notebook, Pocket Size)
 - Hookswitch
 - Dial Pulsing
 - Ground Start
 - Ringer Injection
- Instrumentation
 - Multiplexers
 - Data Acquisition
 - Electronic Switching
 - I/O Subsystems
 - Meters (Watt-Hour, Water, Gas)
- Medical Equipment-Patient/Equipment Isolation
- Security
- Aerospace
- Industrial Controls

Description

PLA110L is a 1-Form-A solid state relay which uses optically coupled MOSFET technology to provide 3750V of input to output isolation. The efficient current limited MOSFET switches and photovoltaic die use Clare's patented OptoMOS® architecture. The optically-coupled input is controlled by a highly efficient GaAlAs infrared LED. The PLA110L can be used to replace mechanical relays and offers the superior reliability associated with semiconductor devices. Because they have no moving parts, they can offer faster, bounce-free switching in a more compact surface mount or through hole package.

Approvals

- UL Recognized: File Number E76270
- CSA Certified: File Number LR 43639-10
- BSI Certified:
 - BS EN 60950:1992 (BS7002:1992) Certificate #:7344
 - BS EN 41003:1993 Certificate #:7344

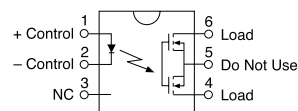
Ordering Information

Part #	Description
PLA110L	6 Pin Dip (50/Tube)
PLA110LS	6 Pin Surface Mount (50/Tube)
PLA110LSTR	6 Pin Surface Mount (1000/Reel)

Pin Configuration

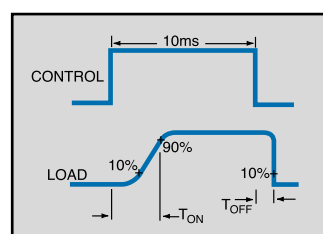
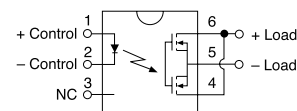
PLA110L Pinout

AC/DC Configuration



PLA110L Pinout

DC Only Configuration



**Absolute Maximum Ratings (@ 25° C)**

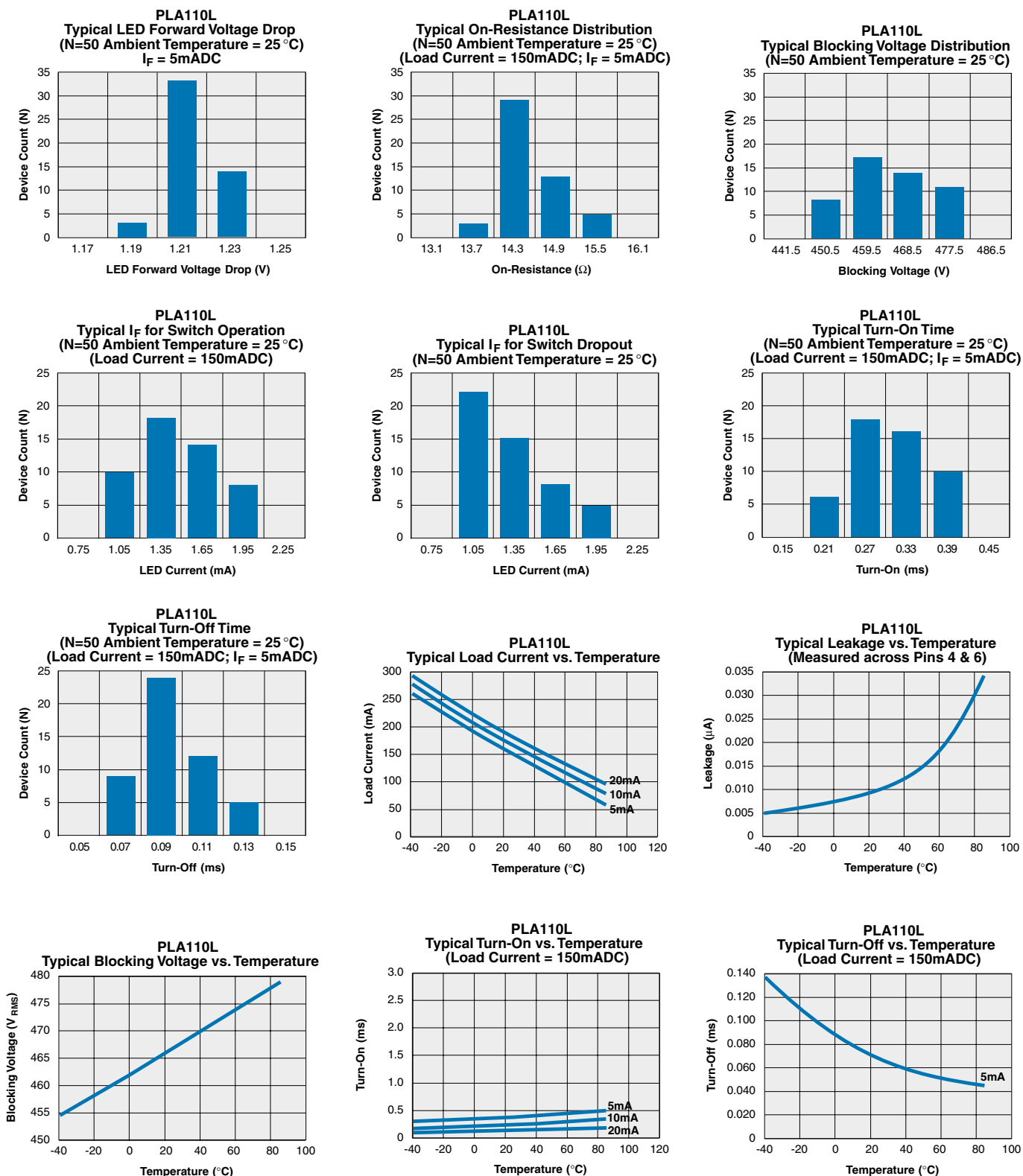
Parameter	Min	Typ	Max	Units
Input Power Dissipation	-	-	150 ¹	mW
Input Control Current	-	-	50	mA
Peak (10ms)	-	-	1	A
Reverse Input Voltage	-	-	5	V
Total Power Dissipation	-	-	800 ²	mW
Isolation Voltage Input to Output	3750	-	-	V _{RMS}
Operational Temperature	-40	-	+85	°C
Storage Temperature	-40	-	+125	°C
Soldering Temperature DIP Package	-	-	+260	°C
Surface Mount Package (10 Seconds Max.)	-	-	+220	°C

¹ Derate Linearly 1.33 mW/°C² Derate Linearly 6.67 mW/°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and effect its reliability.

Electrical Characteristics

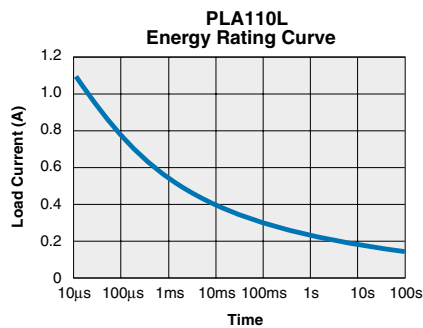
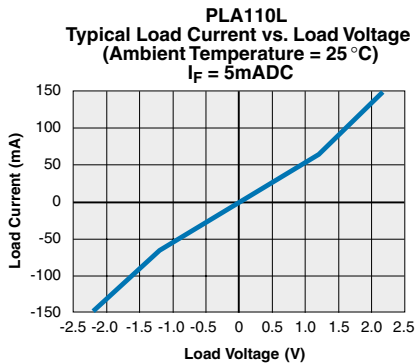
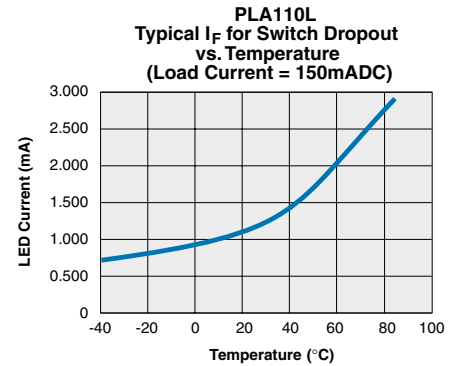
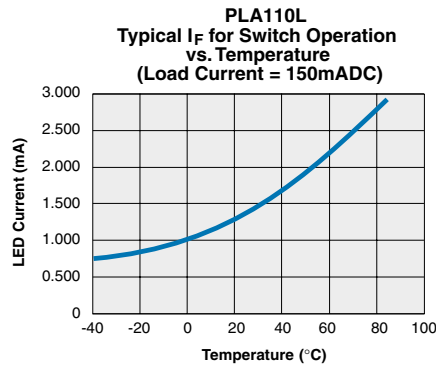
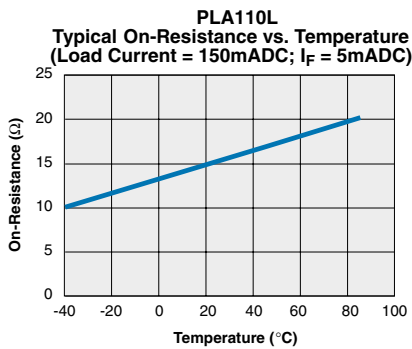
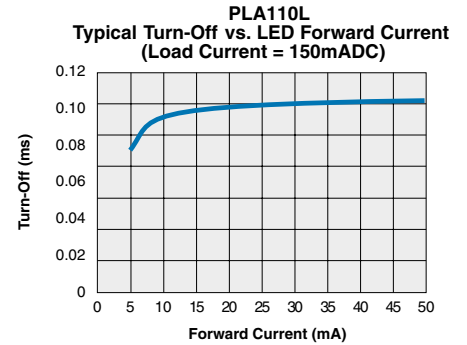
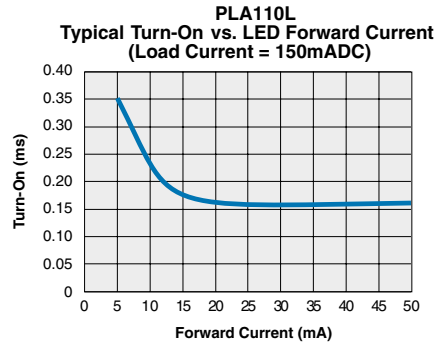
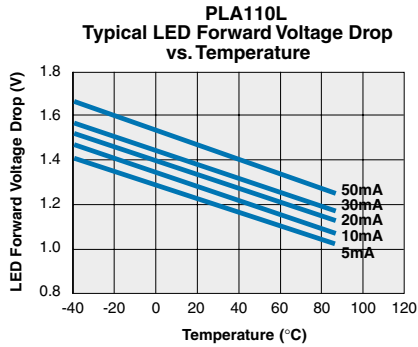
Parameter	Conditions	Symbol	Min	Typ	Max	Units
Output Characteristics @ 25°C						
Load Voltage (Peak)	-	V _L	-	-	400	V
Load Current (Continuous)	-	I _L	-	-	150	mA
AC/DC Configuration	-	I _L	-	-	250	mA
DC Configuration	-	I _L	-	-	-	mA
Peak Load Current	10ms	I _L	-	-	-	mA
On-Resistance	I _L =150mA	R _{ON}	-	-	25	Ω
AC/DC Configuration	I _L =250mA	R _{ON}	-	-	9	Ω
DC Configuration	I _L =250mA	R _{ON}	-	-	9	Ω
Off-State Leakage Current	V _L =400V	I _{LEAK}	-	-	-	μA
Switching Speeds	I _F =5mA, V _L =10V	T _{ON}	-	-	1	ms
Turn-On	I _F =5mA, V _L =10V	T _{OFF}	-	-	0.25	ms
Turn-Off	I _F =5mA, V _L =10V	T _{OFF}	-	-	0.25	ms
Output Capacitance	50V; f=1MHz	C _{OUT}	-	25	-	pF
Load Current Limiting		I _{CL}	190	235	280	mA
Input Characteristics @ 25°C						
Input Control Current	I _L =150mA	I _F	5	-	50	mA
Input Dropout Current	-	I _F	0.4	0.7	-	mA
Input Voltage Drop	I _F =5mA	V _F	0.9	1.2	1.4	V
Reverse Input Voltage	-	V _R	-	-	5	V
Reverse Input Current	V _R =5V	I _R	-	-	10	μA
Common Characteristics @ 25°C						
Input to Output Capacitance	-	C _{I/O}	-	3	-	pF
Input to Output Isolation	-	V _{I/O}	3750	-	-	V _{RMS}

PERFORMANCE DATA*


*The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.

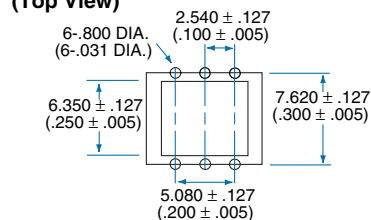


PERFORMANCE DATA*

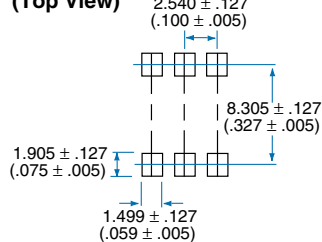


*The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.

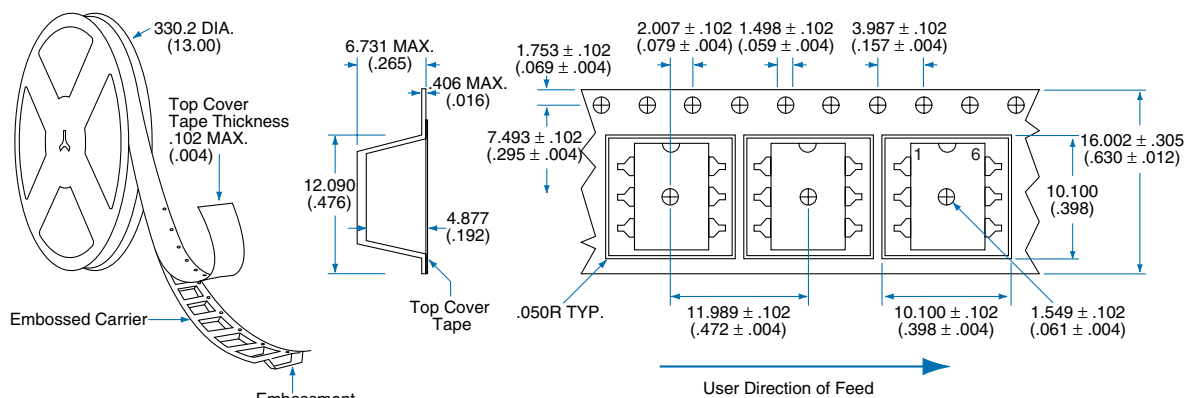
6 Pin DIP Through Hole (Standard)



6 Pin DIP Surface Mount (“S” Suffix)



Tape and Reel Packaging for 6 Pin Surface Mount Package



Rev. 4.0



CLARE

For additional information please visit our website at: www.clare.com

Clare, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. Neither circuit patent licenses nor indemnity are expressed or implied. Except as set forth in Clare's Standard Terms and Conditions of Sale, Clare, Inc. assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

The products described in this document are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or where malfunction of Clare's product may result in direct physical harm, injury, or death to a person or severe property or environmental damage. Clare, Inc. reserves the right to discontinue or make changes to its products at any time without notice.

Specification: DS-PLA110L-R4.0
©Copyright 2002, Clare, Inc.
OptoMOS® is a registered trademark of Clare, Inc.
All rights reserved. Printed in USA.
6/21/02