PIC32MX3/4 Family Rev. B3 Silicon Errata

The PIC32MX3/4 devices (Rev. B3) you received conform functionally to the corresponding device data sheet (DS61143**D**) and family reference manual (DS61132**B**), except for the anomalies described in this silicon errata document.

Any data sheet or reference manual clarification issues related to the PIC32MX3/4 family would be described in an errata document and made available on the Microchip web site, www.microchip.com.

Silicon errata listed in this document are pertinent exclusively to PIC32MX3/4 family devices with the following Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC32MX440F256H	0x52	0x409
PIC32MX440F512H	0x56	0x409
PIC32MX440F128H	0x4D	0x409
PIC32MX360F512L	0x38	0x409
PIC32MX360F256L	0x34	0x409
PIC32MX340F128L	0x2D	0x409
PIC32MX320F128L	0x2A	0x409
PIC32MX340F512H	0x16	0x409
PIC32MX340F256H	0x12	0x409
PIC32MX340F128H	0x0D	0x409
PIC32MX320F128H	0x0A	0x409
PIC32MX320F064H	0x06	0x409
PIC32MX320F032H	0x02	0x409

The Device and Revision IDs of a PIC32MX3/4 device can be identified by performing a “Reset and Connect” operation to the device using MPLAB® REAL ICE™ in-circuit emulator with MPLAB IDE, version 8.0 or later.

“Reset and Connect” requires that a device is specified by clicking *Configure>Select Device*. A message that includes the Device ID Revision number of the device is displayed in the **Output** window to indicate successful connection to the device.

A Device ID Revision number acquired by this method can be resolved to the data in the preceding table by splitting the number, as demonstrated by the following example:

“Device ID Revision = 40938000” yields the following IDs:

Device ID = 0x38
Revision ID = 0x409

The errata described in this document will be addressed in future revisions of the silicon.

1. Module: Device Reset

A Reset ($\overline{MCLR}$) Pulse that is shorter than 2 SYSCLK will not reset the device properly.

Work around

Ensure that the device is held in Reset for more than 2 SYSCLK to ensure proper device Reset operation.

2. Module: Device Reset

All Resets, except Power-on Reset (POR), can cause a Fail-Safe Clock Monitor event (if enabled) when the duration of the Reset pulse exceeds the clock period of the internal fail-safe clock reference clock – 31 kHz.

Work around

If long Reset pulses are anticipated, ignore or disable Fail-Safe Clock Monitor events.

3. Module: Software Device Reset

Attempting to perform a software device Reset with PBDIV set to 1:1, and SYSCLK less than 1 MHz will not reset the device properly.

Work arounds

Work around 1:

Change PBDIV before performing a software Reset.

Work around 2:

Set SYSCLK to a value that is greater than 1 MHz.

4. Module: External Voltage Regulator Mode

A V_{DDCORE} voltage less than 1.75V will cause the CPU to reset when using an external core voltage supply.

Work arounds

Work around 1:

Use the internal voltage regulator.

Work around 2:

Use an external 1.8V regulator which has a regulation specification of <= 2.5%. The Microchip TC1055-1.8VCT713 Low Drop-Out (LDO) regulator, or an equivalent, is recommended.

5. Module: ADC

When running the A/D converter in Internal Reference mode, the gain error is 3-4 LSb and the offset error is 1-2 LSb across voltage and speed.

Work around

Use in-system calibration and software techniques to compensate for these errors.

6. Module: Bus Matrix Registers

BMXDUDBA, BMXDUPBA, and BMXPUPBA registers can be set to values that are outside the device's actual memory-size limit.

Work around

Do not write values greater than the specified memory size of the device to the Bus Matrix registers. Ensure that the upper bits of the registers remain clear ('0').

7. Module: Clock Failure Event

After a clock failure event, any write to the OSCCON register erroneously clears the fail-safe condition and attempts to switch to a new clock source that is specified by the NOSC bits in the OSCCON register.

Work around

After a clock failure event, perform the following steps:

1. Write '000' to the NOSC bits in the OSCCON register to select the Fast RC oscillator. This will ensure that an erroneous clock switch selects the known good on-chip Fast RC oscillator.
2. Modify the OSCCON register with any value your application requires.

8. Module: DMA Pattern Match Mode

In Pattern Match mode, the DMA will generate up to 3 additional byte writes to the destination address, after the Pattern Detection event has occurred when performing transfers with the DCHxSSIZ set to greater than 1.

Work arounds

Work around 1:

The destination buffer needs to be large enough to accommodate the extra bytes (up to 3 extra bytes).

Work around 2:

Set the destination size register to 1.

Work around 3:

Set the source size register to 1.

9. Module: Output Compare in PWM Mode

The Output Compare module in PWM mode outputs a high of period register (PRx) length when attempting to use PWM values of 0x00 followed by 0x01.

Work around

Do not use a PWM value of 0x01.

10. Module: Parallel Master Port (PMP)

In PMP Slave 4B Buffer mode, if the underflow Status bit OBF (PMSTAT<6>) is cleared at the same time that a PMP read is attempted, the PMP could get incorrect data.

Work around

The CPU can read the underflow flag OBUF and set/clear an I/O pin for the external master device to read. The state of the pin should indicate to the external master device that an underflow has occurred and no additional reads should occur until the underflow status has been cleared by the CPU.

11. Module: PORTs

When using hardware assisted read-modify-write registers, PORTxINV/PORTxSET/PORTxCLR, the source used for the operation is the LATx register, not the PORTx register. This only affects users who wish to use the pins in a bi-directional mode or wish to store sampled PORTx data in the LATx register.

Work around

Use a software read-modify-write sequence, such as:

```
//replaces PORTAINV = mask;
x = PORTA ^ mask;
LATA = x;

//replaces PORTASET = mask;
x = PORTA | mask;
LATA = x;

//replaces PORTACLR = mask;
x = PORTA & ~mask;
LATA = x;
```

Note: These sequences are not atomic.

12. Module: Timer1, 2, 3, 4, 5

The TMRx register stays at zero for two timer clock cycles when the PRx register is 0x0000.

Work around

None.

13. Module: Timer1, 2, 3, 4, 5

Writes to the SET/CLR/INV registers for TMRx and PRx produce incorrect results.

Work around

Use TMRx and PRx registers to manipulate bits. Use a software read-modify-write sequence; e.g.,

```
TMR1 = TMR1 | 0x8000;
```

14. Module: Timer1 in Asynchronous Mode

The Timer1 prescaler may not be reset correctly when it is used with a slow external clock. This can occur when the timer is disabled and then re-enabled. The result could be a spurious count in the prescaler.

Work around

None.

15. Module: UART Hardware Handshake Mode

The CTS pin does not deassert until at least 2 bytes are free in the UART FIFO.

Work around

The UART TXREG must be read at least 2 times to rearm the hardware handshaking lines.

16. Module: Watchdog Timer (WDT)

An incorrect WDT time-out Reset may occur when both of these conditions are present:

1. WDT is enabled.
2. Either a $\overline{\text{MCLR}}$ (EXTR) or Software Reset (SWR) occurs just before WDT is about to expire.

Work around

To detect incorrect WDT time-out Reset, always confirm that only the WDTO bit is set in RCON register. If EXTR, SWR, or any other Reset bits are set, it indicates that an incorrect WDT has occurred.

17. Module: DMA Channel Abort

DMA channel abort on a channel that is not currently active may have unintended effects on other active channels.

Work around

1. Suspend the channel, rather than abort, by clearing the channel enable bit DCHxCON<CHEN>.
2. Wait until other DMA channels complete before issuing the abort.

18. Module: Oscillator

The Primary Oscillator Circuit (POSC), when using XT/XTPLL/HS/HSPLL modes, does not operate over the voltage and temperature range that is listed as item D5 in the device data sheet. The operation range without the work around is limited to -40°C through +70°C when V_{DD} <3.0V.

Work around

Install a 4.1 MΩ resistor in parallel with the crystal. This allows operation across the temperature range that is listed in the data sheet.

19. Module: Parallel Master Port (PMP)

The WAITE field in PMMODE<1:0> does not add a Wait state to PMP master reads when it is programmed to the value '01'. The WAITE field allows Wait states to be added to the end of PMP read/write operations. This field is intended to add the following Wait clocks after the read operation completes:

00 – no Wait states
01 – 1 Wait state
10 – 2 Wait states
11 – 3 Wait states

Current behavior is the following:

00 – no Wait states
01 – no Wait states
10 – 2 Wait states
11 – 3 Wait states

Work around

This erratum only applies to PMP master read operations. PMP writes work correctly. Use another wait state control value that is allowed for the attached device.

20. Module: UART Baud Rate Generator

Using BRG values of 0, 1, or 2 cause the Start bit to be shortened. This results in errors when receiving the data. This issue exists for BRGH values of '0' and '1'

Work around

Do not use BRG values of 0, 1, or 2. Select system and peripheral bus clocks' frequencies such that the BRG value for the desired baud rate generator value is greater than 2.

21. Module: Input Capture with DMA in 16-Bit Mode

16-bit DMA transfers from the ICAP module FIFO buffer do not advance the ICAP FIFO pointer. This results in the entire DMA output buffer being filled with the first value from the ICAP FIFO.

Work around

Configure the DMA to perform 32-bit transfers from the ICAP FIFO.

22. Module: USB

The D plus and D minus pins are not 5V tolerant. During normal operation these pins are not subject to 5V. The 5V tolerance specification is intended to prevent device damage in an abnormal operation mode such as connecting a shorted USB cable to the device.

Work around

Do not subject D plus or D minus to 5V.

23. Module: USB Module Cannot Communicate in Host Mode with a Low-Speed Device Connected Through a Hub

The USB module does not correctly switch from full speed to low speed after sending a PRE packet to a hub.

Work around

Connect a low-speed device directly to the PIC32.

24. Module: Breakpoints While Using DMA

The DMA buffer may be erroniously filled with the last data read prior to the breakpoint. This buffer fill will continiue until the DMA buffer is full.

However, the DMA buffer fills correctly if those same peripherals are used as DMA destinations, even when the CPU goes into Debug Exception mode.

This behavior occurs when the DMA controller is actively transferring data and a debugger hits a breakpoint, causes a single-step operation, or halts the target. See Table 1.

The following table lists the peripherals and input registers that could affect DMA buffer usage.

TABLE 1: REGISTERS AND PERIPHERALS AFFECTED BY BREAKPOINTS DURING DMA TRANSFERS

Peripheral as DMA Source	Transfer from Input Register
Change Notice	PORTx
SPI	SPIxBUF
PMP	PMDIN
UART	UxRXREG
Input Capture	ICxBUF

Work around

If the debugger halts during a DMA transfer from one of these registers, either ignore the DMA transferred data or restart the debug session.

25. Module: Using PMP as DMA source

Events can be missed if the PMDIN register is used as the DMA source and the PMP IRQ is used as the DMA trigger.

Work around

Do not use DMA for PMP read operations. DMA can be used for PMP write operations with the PMDIN register as the DMA destination.

26. Module: USB Single-Ended Comparator Trip Point Violates USB Specification

The single-ended comparator used to detect SE0 transitions at a voltage higher than the USB specification. This is a compliance issue relating to items ST2 and ST3 in the Peripheral Silicon checklist. This may result in reduced noise immunity.

Work around

None.

27. Module: Input Capture

When in 16-bit mode, the upper 16 bits of the 32-bit ICxBUF register contain Timer3 values.

Work around

Mask the upper 16 bits of the read value.

Example: result = 0xFFFF & IC1BUF

28. Module: 2-Wire Programming

When programming the PIC32 using the 2-wire PGC and PGD pins, programming data appears as an output on the JTAG TDO pin.

Work around

Do not connect the TDO pin to a device that would be adversely affected by rapid pin toggling during programming.

APPENDIX A: REVISION HISTORY

Revision A (02/2008)

Initial release of this document.

Revision B (04/2008)

Oscillator temperature issue was added. Flash Program Memory 500ns delay requirement is now classified as architectural behavior. Added PMP WAITE behavior.

Revision C (10/2008)

Modified errata item 11 PORTs. Added errata items 20 UART module, 21 Input Capture module, 22 USB module, 23 USB module, 24 Breakpoints, 25 Parallel Master Port module, 26 Parallel Master Port module, 27 USB module, 28 Input Capture module and 29 2-Wire Programming.

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