PIC24FJ256GB110 FAMILY

PIC24FJ256GB110 Family Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39897**B**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC24FJ256GB110 family will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Electrical Characteristics

The following tables are changed with the new or modified values shown in bold text:

- Table 28-4:
  DC Characteristics: Operating Current (I_{DD})
- Table 28-5:
  DC Characteristics: Idle Current (I_{IDLE})
- Table 28-6:
  DC Characteristics: Power-Down Current (I_{PD})

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TABLE 28-4: DC CHARACTERISTICS: OPERATING CURRENT (I$_{DD}$)

DC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T$_A$ ≤ +85°C for Industrial		
Parameter No.	Typical[1]	Max	Units	Conditions		
Operating Current (I$_{DD}$)[2]						
DC20	0.83	1.2	mA	-40°C	2.0V[3]	1 MIPS
DC20a	0.83	1.2	mA	+25°C		
DC20b	0.83	1.2	mA	+85°C		
DC20d	1.1	**1.7**	mA	-40°C	3.3V[4]	
DC20e	1.1	**1.7**	mA	+25°C		
DC20f	1.1	**1.7**	mA	+85°C		
DC23	3.3	**4.5**	mA	-40°C	2.0V[3]	4 MIPS
DC23a	3.3	**4.5**	mA	+25°C		
DC23b	3.3	**4.6**	mA	+85°C		
DC23d	4.3	6.0	mA	-40°C	3.3V[4]	
DC23e	4.3	6.0	mA	+25°C		
DC23f	4.3	6.0	mA	+85°C		
DC24	18.2	24.0	mA	-40°C	2.5V[3]	16 MIPS
DC24a	18.2	24.0	mA	+25°C		
DC24b	18.2	24.0	mA	+85°C		
DC24d	18.2	24.0	mA	-40°C	3.3V[4]	
DC24e	18.2	24.0	mA	+25°C		
DC24f	18.2	24.0	mA	+85°C		
DC31	15.0	**35.0**	μA	-40°C	2.0V[3]	LPRC (31 kHz)
DC31a	15.0	**35.0**	μA	+25°C		
DC31b	20.0	**50.0**	μA	+85°C		
DC31d	57.0	75.0	μA	-40°C	3.3V[4]	
DC31e	57.0	75.0	μA	+25°C		
DC31f	95.0	124.0	μA	+85°C		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all I$_{DD}$ measurements are as follows: OSCI driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to V$_{DD}$. $\overline{MCLR}$ = V$_{DD}$; WDT and FSCM are disabled. CPU, SRAM, program memory and data memory are operational. No peripheral modules are operating and all of the Peripheral Module Disable (PMD) bits are set.

3: On-chip voltage regulator disabled (ENVREG tied to V$_{SS}$).

4: On-chip voltage regulator enabled (ENVREG tied to V$_{DD}$), Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

TABLE 28-5: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C $\leq$ TA $\leq$ +85°C for Industrial		
Parameter No.	Typical[1]	Max	Units	Conditions		
Idle Current (I_{IDLE}**)**[2]						
DC40	220	**310**	µA	-40°C	2.0V[3]	1 MIPS
DC40a	220	**310**	µA	+25°C		
DC40b	220	**310**	µA	+85°C		
DC40d	300	390	µA	-40°C	3.3V[4]	
DC40e	300	390	µA	+25°C		
DC40f	320	420	µA	+85°C		
DC43	0.85	1.1	mA	-40°C	2.0V[3]	4 MIPS
DC43a	0.85	1.1	mA	+25°C		
DC43b	0.87	1.2	mA	+85°C		
DC43d	1.1	1.4	mA	-40°C	3.3V[4]	
DC43e	1.1	1.4	mA	+25°C		
DC43f	1.1	1.4	mA	+85°C		
DC47	4.4	5.6	mA	-40°C	2.5V[3]	16 MIPS
DC47a	4.4	5.6	mA	+25°C		
DC47b	4.4	5.6	mA	+85°C		
DC47c	4.4	5.6	mA	-40°C	3.3V[4]	
DC47d	4.4	5.6	mA	+25°C		
DC47e	4.4	5.6	mA	+85°C		
DC50	1.1	1.4	mA	-40°C	2.0V[3]	FRC (4 MIPS)
DC50a	1.1	1.4	mA	+25°C		
DC50b	1.1	1.4	mA	+85°C		
DC50d	1.4	1.8	mA	-40°C	3.3V[4]	
DC50e	1.4	1.8	mA	+25°C		
DC50f	1.4	1.8	mA	+85°C		
DC51	4.3	6.0	µA	-40°C	2.0V[3]	LPRC (31 kHz)
DC51a	4.5	6.0	µA	+25°C		
DC51b	**10.0**	25	µA	+85°C		
DC51d	**44.0**	**60.0**	µA	-40°C	3.3V[4]	
DC51e	44.0	**60.0**	µA	+25°C		
DC51f	70.0	**115.0**	µA	+85°C		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

    2: Base I_{IDLE} current is measured with core off, OSCI driven with external square wave from rail to rail. All I/O pins are configured as inputs and pulled to V_{DD}. $\overline{\text{MCLR}}$ = V_{DD}; WDT and FSCM are disabled. No peripheral modules are operating and all of the Peripheral Module Disable (PMD) bits are set.

    3: On-chip voltage regulator disabled (ENVREG tied to V_{SS}).

    4: On-chip voltage regulator enabled (ENVREG tied to V_{DD}), Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

TABLE 28-6: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial		
Parameter No.	Typical[1]	Max	Units	Conditions		
Power-Down Current (IPD)[2]						
DC60	0.1	1.0	μA	-40°C	2.0V[3]	Base Power-Down Current[5]
DC60a	0.15	1.0	μA	+25°C		
DC60b	3.7	18.0	μA	+85°C		
DC60c	0.2	**1.4**	μA	-40°C	2.5V[3]	
DC60d	0.25	**1.4**	μA	+25°C		
DC60e	4.2	27.0	μA	+85°C		
DC60f	3.6	**10.0**	μA	-40°C	3.3V[4]	
DC60g	4.0	10.0	μA	+25°C		
DC60h	11.0	36.0	μA	+85°C		
DC61	1.75	3	μA	-40°C	2.0V[3]	Watchdog Timer Current: ΔIWDT[5]
DC61a	1.75	3	μA	+25°C		
DC61b	1.75	3	μA	+85°C		
DC61c	2.4	4	μA	-40°C	2.5V[3]	
DC61d	2.4	4	μA	+25°C		
DC61e	2.4	4	μA	+85°C		
DC61f	2.8	5	μA	-40°C	3.3V[4]	
DC61g	2.8	5	μA	+25°C		
DC61h	2.8	5	μA	+85°C		
DC62	2.5	7.0	μA	-40°C	2.0V[3]	RTCC + Timer1 w/32 kHz Crystal: ΔRTCC + ΔITI32[5]
DC62a	2.5	7.0	μA	+25°C		
DC62b	3.0	7.0	μA	+85°C		
DC62c	2.8	7.0	μA	-40°C	2.5V[3]	
DC62d	3.0	7.0	μA	+25°C		
DC62e	3.0	7.0	μA	+85°C		
DC62f	3.5	10.0	μA	-40°C	3.3V[4]	
DC62g	3.5	10.0	μA	+25°C		
DC62h	4.0	10.0	μA	+85°C		

Note 1: Data in the Typical column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled high. WDT, etc., are all switched off, and the Peripheral Module Disable (PMD) bits for all unused peripherals are set.

3: On-chip voltage regulator disabled (ENVREG tied to VSS).

4: On-chip voltage regulator enabled (ENVREG tied to VDD), Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

5: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

REVISION HISTORY

<u>Rev A Document (7/2008)</u>
Initial release of this data sheet errata. Incudes Data
Sheet Clarification 1 (Electrical Characteristics).

NOTES:

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