PIC18F2220/2320/4220/4320 Rev. B3 Silicon/Data Sheet Errata

The PIC18F2220/2320/4220/4320 Rev. B3 parts you have received conform functionally to the Device Data Sheet (DS39599**C**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC18F2220/2320/4220/4320 silicon.

The following silicon errata apply only to PIC18F2220/2320/4220/4320 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2220	00 0101 100	0 0100
PIC18F2320	00 0101 000	0 0100
PIC18F4220	00 0101 101	0 0100
PIC18F4320	00 0101 001	0 0100

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Internal Oscillator Block

If the INTRC clock source was not started at POR (any VDD) and VDD is greater than 4.5V, the INTRC clock source may not start or may require a long delay when starting. The INTRC may not restart when VDD is lowered below 4.5V.

Features that depend on the operation of the INTRC clock source may be affected. These include the INTOSC output when exiting from Sleep mode, the Watchdog Timer (WDT) if enabled by firmware using the WDTCON register, Two-Speed Start-ups during Reset or wake-up from Sleep and the Fail-Safe Clock Monitor (FSCM) when exiting Sleep mode.

The INTOSC frequency may rise very high (for example, 9.5 MHz). The WDT and the FSCM may simply not function. Two-Speed Start-ups may not occur, but execution will start once the primary clock source becomes ready.

Work around

Several work arounds may be used.

1. Enable the WDT in Configuration register, CONFIG2H and place a `CLRWDT` instruction somewhere in the main loop.
2. Configure the internal oscillator block as the primary clock source using Configuration Register 1H.
3. Any technique that starts the INTRC at Reset and does not disable it may be used.
4. Ensure that VDD is below 4.5V when starting the INTRC clock source.

There may be other work arounds.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Core (`DAW` Instruction)

The `DAW` instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the `DAW` instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as `INCFSZ` (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the `DAW` instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB

This is repeated for each DAW instruction.
```

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Internal Oscillator Block

At high temperature (above 85°C) or low VDD (below 2.5V), the IOFS bit (OSCCON<2>) may not become set when the internal oscillator block is selected as the system clock source for any frequency above 31 kHz (OSCCON<6:4> ≠ 000). The INTOSC output will stabilize at 8 MHz; however, the IOFS bit may not become set.

Work around

If time critical code is to be executed, it should be delayed by 1 ms following the operation that enables the 8 MHz INTOSC output from the internal oscillator block.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: INTOSC

Incrementing or decrementing the value in the OSCTUNE register may not have the expected effect of shifting the INTRC or INTOSC output frequencies. The OSCTUNE values beyond which this happens may vary with temperatures above 70°C.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: MSSP (All I²C™ and SPI™ Modes)

The Buffer Full flag bit (BF) of the SSPSTAT register (SSPSTAT<0>) may be inadvertently cleared, even when the SSPBUF register has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111) and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

Identified work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh.

In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select all GPR Banks.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain C9h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: MSSP (SPI, Slave Mode)

In its current implementation, the $\overline{SS}$ (Slave Select) control signal generated by an external master processor may not be successfully recognized by the PIC® microcontroller operating in Slave Select mode (SSPM3:SSPM0 = 0100). In particular, it has been observed that faster transitions (those with shorter fall times) are more likely to be missed than slower transitions.

Work around

Insert a series resistor between the source of the $\overline{SS}$ signal and the corresponding $\overline{SS}$ input line of the microcontroller. The value of the resistor is dependent on both the application system's characteristics and process variations between microcontrollers. Experimentation and thorough testing is encouraged.

This is a recommended solution; others may exist.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: Data EEPROM

When writing to the data EEPROM, the contents of the data EEPROM memory may not be written as expected.

Work around

Either of two work arounds can be used:

1. Before beginning any writes to the data EEPROM, enable the LVD (any voltage) and wait for the internal voltage reference to become stable. LVD interrupt requests may be ignored. Once the LVD voltage reference is stable, perform all EEPROM writes normally. When writes have been completed, the LVD may be disabled.
2. Configure the BOR as enabled (any voltage). Select a threshold below V_{DD} to allow normal operation. If V_{DD} is below the BOR threshold, the device will be held in BOR Reset.

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet

In the Device Data Sheet (DS39599**C**), the following clarifications and corrections should be noted.

1. Module: RE3 Pin (PORTE<3>)

RE3 (PORTE<3>) is NOT available as an input in PIC18F2220 and PIC18F2320 devices when MCLR has been disabled in CONFIG3H<7>.

In 28-pin devices, RE3 (and all PORTE bits) always reads back as '0'. The MCLR Reset can be enabled/disabled using the MCLRE bit (CONFIG3H<7>). When the MCLR Reset is disabled, the MCLR/VPP pin should not be allowed to float and can be pulled to VDD or VSS using a 1K to 10K resister (an existing MCLR circuit satisfies this requirement). Device programming is not affected by the setting of MCLRE.

The following table lists the data sheet changes related to this issue.

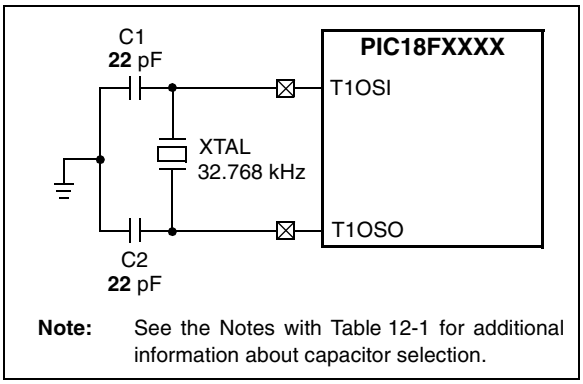
TABLE 1: DEVICE DATA SHEET CHANGES

Item	Page Number	Description
Pin Diagrams	2	The pin name RE3 has been deleted from pin location 1 in the 28-pin SPDIP and SOIC package diagram.
Figure 1-1	9	PORTE and **Note 2** have been deleted from the PIC18F2220/2320 Block Diagram.
Table 1-2	11, 13	RE3 information has been deleted.
Table 5-1	61	**Note 2** is added to PORTE.
Table 5-2	64	**Note 5** has been changed to: These registers and/or bits are not implemented on the PIC18F2X20 devices and read as 0x00. **Note 5** designation has been removed from the following bits: TRISE<2:0> and PORTE<2:0> and added to File Names: PORTE and PORTD. **Note 6** has been changed to: The RE3 port bit is only available as an input-only pin in 40-pin devices when Master Clear functionality is disabled (CONFIG3H<7> = 0).
Section 10.5	111	The first paragraph has been changed to read: PORTE is only available in PIC18F4X20 devices. PIC18F2X20 devices will always read back 0x00 from PORTE.
Section 10.5.1	111	This section heading and the following paragraph have been removed.
Table 10-9	113	**Note 2** has been added to MCLR/VPP/RE3, which reads: The RE3 port bit is only available as an input-only pin in 40-pin devices when Master Clear functionality is disabled (CONFIG3H<7> = 0).
Table 10-10	113	**Note 1** has been changed to read: The RE3 port bit is only available as an input-only pin in 40-pin devices when Master Clear functionality is disabled (CONFIG3H<7> = 0).
Table 19-2	220	**Note 1** has been changed to read: The RE3 port bit is only available as an input-only pin in 40-pin devices when Master Clear functionality is disabled (CONFIG3H<7> = 0). **Note 2** on bit 3 (RE3) in register PORTE has been replaced with **Note 1**. **Note 3** on registers TRISE and LATE has been replaced with **Note 2**, which now reads: This register is not implemented on PIC18F2X20 devices and reads back 0x00. This note should also be added to register PORTE. **Note 3** has been removed. **Note 4** is now **Note 3**.
Register 23-4	240	The text for value 0 in bit 7 (MCLRE) has been changed to: 0 = MCLR disabled; RE3 input pin is enabled in 40-pin devices only (PIC18F4X20).

2. Module: Timer1 Oscillator

In **Section 12.2 "Timer1 Oscillator"**, capacitor values for C1 and C2 were incorrectly specified in Figure 12-3 and Table 12-1. The correct values are shown in bold:

FIGURE 12-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR



Note: See the Notes with Table 12-1 for additional information about capacitor selection.

TABLE 12-1: CAPACITOR SELECTION FOR THE TIMER OSCILLATOR(2,3,4)

Osc Type	Freq	C1	C2
LP	32 kHz	**22** pF(1)	**22** pF(1)

Note 1: Microchip suggests this value as a starting point in validating the oscillator circuit.

2: Higher capacitance increases the stability of the oscillator but also increases the start-up time.

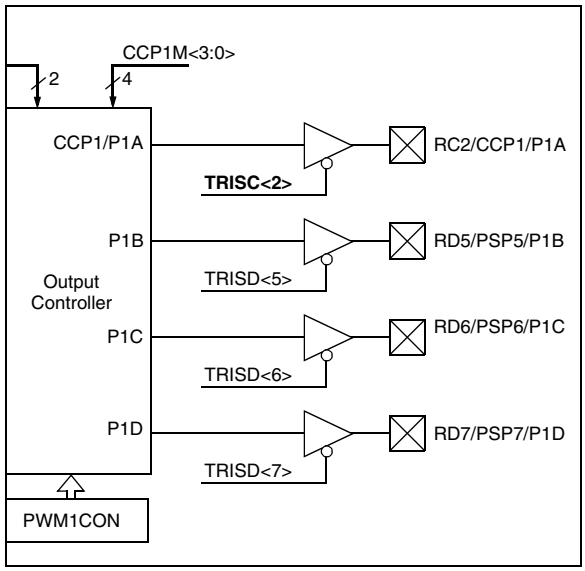
3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Capacitor values are for design guidance only.

3. Module: Enhanced PWM Module Block Diagram

In **Section 16.4 "Enhanced PWM Mode",** the incorrect TRIS bit (TRISD<4>) is specified in Figure 16-1 for RC2/CCP1/P1A. The correct bit is TRISC<2>. The correction is shown in bold text (only the affected area of the block diagram is shown to conserve space).

FIGURE 16-1: SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODULE



4. Module: Enabling SPI I/O

In **Section 17.3.3 "Enabling SPI I/O",** the incorrect TRIS bit (TRISC<5>) is specified for Slave Select ($\overline{SS}$). The correct bit is TRISA<5>. The correction is shown in bold text.

17.3.3 ENABLING SPI I/O

To enable the serial port, SSP Enable bit, SSPEN (SSPCON1<5>), must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCON registers and then set the SSPEN bit. This configures the SDI, SDO, SCK and $\overline{SS}$ pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- SDI must have TRISC<4> bit cleared
- SDO must have TRISC<5> bit cleared
- SCK (Master mode) must have TRISC<3> bit cleared
- SCK (Slave mode) must have TRISC<3> bit set
- $\overline{SS}$ must have **TRISA<5>** bit set

5. Module: DC Characteristics

The specifications and parameter numbers for the Brown-out Voltage limits (V_{BOR}, originally parameters D005 and D005E) in **Section 26.1 "DC Characteristics: Supply Voltage"** of the Device Data Sheet have been changed.

The specifications and parameter numbers have been revised for devices with date codes from 0351xxx to 0417xxx, inclusive.

Specifications and parameter numbers have been revised for specific temperature ranges for date codes from 0418xxx and higher.

The new information is shown in bold text.

26.1 DC Characteristics: Supply Voltage PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial)

PIC18LF2220/2320/4220/4320 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2220/2320/4220/4320 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Date Codes from 0351xxx to 0417xxx, inclusive							
D005A	V_{BOR}	**Brown-out Reset Voltage**					
		PIC18LF2X20/4X20	Industrial Low Voltage **(-40°C to +85°C)**				
		BORV1:BORV0 = 11	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 10	**2.45**	**2.72**	**2.99**	V	
		BORV1:BORV0 = 01	**3.80**	**4.22**	**4.64**	V	
		BORV1:BORV0 = 00	**4.09**	**4.54**	**4.99**	V	
D005B		PIC18F2X20/4X20	Industrial **(-40°C to +85°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**3.80**	**4.22**	**4.64**	V	**(Note 2)**
		BORV1:BORV0 = 00	**4.09**	**4.54**	**4.99**	V	**(Note 2)**
D005C		PIC18F2X20/4X20	Extended **(-40°C to +125°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**3.80**	**4.22**	**4.64**	V	**(Note 2)**
		BORV1:BORV0 = 00	**4.09**	**4.54**	**4.99**	V	**(Note 2)**

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which V_{DD} can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: **When BOR is on and BORV<1:0> = 0x, the device will operate correctly at 40 MHz for any V_{DD} at which the BOR allows execution.**

26.1 DC Characteristics: Supply Voltage PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial) (Continued)

PIC18LF2220/2320/4220/4320 (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC18F2220/2320/4220/4320 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Date Codes from 0417xxx and higher							
	VBOR	**Brown-out Reset Voltage**					
D005D		PIC18LF2X20/4X20	Industrial Low Voltage **(-10°C to +85°C)**				
		BORV1:BORV0 = 11	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 10	**2.50**	**2.72**	**2.94**	V	
		BORV1:BORV0 = 01	**3.88**	**4.22**	**4.56**	V	
		BORV1:BORV0 = 00	**4.18**	**4.54**	**4.90**	V	
D005F		PIC18LF2X20/4X20	Industrial Low Voltage **(-40°C to -10°C)**				
		BORV1:BORV0 = 11	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 10	**2.34**	**2.72**	**3.10**	V	
		BORV1:BORV0 = 01	**3.63**	**4.22**	**4.81**	V	
		BORV1:BORV0 = 00	**3.90**	**4.54**	**5.18**	V	
D005G		PIC18F2X20/4X20	Industrial **(-10°C to +85°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**3.88**	**4.22**	**4.56**	V	**(Note 2)**
		BORV1:BORV0 = 00	**4.18**	**4.54**	**4.90**	V	**(Note 2)**
D005H		PIC18F2X20/4X20	Industrial **(-40°C to -10°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 00	**3.90**	**4.54**	**5.18**	V	**(Note 2)**
D005J		PIC18F2X20/4X20	Extended **(-10°C to +85°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**3.88**	**4.22**	**4.56**	V	**(Note 2)**
		BORV1:BORV0 = 00	**4.18**	**4.54**	**4.90**	V	**(Note 2)**
D005K		PIC18F2X20/4X20	Extended **(-40°C to -10°C, +85°C to +125°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 00	**3.90**	**4.54**	**5.18**	V	**(Note 2)**

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: When BOR is on and BORV<1:0> = 0x, the device will operate correctly at 40 MHz for any VDD at which the BOR allows execution.

6. Module: DC Characteristics

Typical values for parameter D022A (Brown-out Reset) and parameter D022B (Low-Voltage Detect) have changed. The new values are shown in bold text.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial)

PIC18LF2220/2320/4220/4320 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2220/2320/4220/4320 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**	
D022A (ΔIBOR)	**Brown-out Reset**	17	35.0	µA	-40°C to +85°C	VDD = 3.0V
		20	45.0	µA	-40°C to +85°C	VDD = 5.0V
	Extended devices only	**24**	50.0	µA	-40°C to +125°C	
D022B (ΔILVD)	**Low-Voltage Detect**	14	25.0	µA	-40°C to +85°C	VDD = 2.0V
		18	35.0	µA	-40°C to +85°C	VDD = 3.0V
		24	45.0	µA	-40°C to +85°C	VDD = 5.0V
	Extended devices only	24	50.0	µA	-40°C to +125°C	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;

$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

7. Module: LVD Characteristics

The specifications and parameter numbers for the Low-Voltage Detect thresholds (V_{LVD}, originally parameters D420 and D420E) in **Section 26.3 "DC Characteristics"** of the Device Data Sheet have been changed.

The specifications and parameter numbers have been revised for devices with date codes from 0351xxx to 0417xxx, inclusive.

Specifications and parameter numbers have been revised for specific temperature ranges for date codes from 0418xxx and higher.

The new information is shown in bold text.

TABLE 26-4: LOW-VOLTAGE DETECT CHARACTERISTICS

PIC18LF2220/2320/4220/4320 (Industrial)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2220/2320/4220/4320 (Industrial, Extended)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
Date Codes from 0351xxx to 0417xxx, inclusive								
D420A	V_{LVD}	LVD Voltage on V_{DD} Transition High-to-Low		Industrial Low Voltage **(-40°C to +85°C)**				
		PIC18LF2X20/4X20	LVDL<3:0> = 0000	**N/A**	**N/A**	**N/A**	V	Reserved
			LVDL<3:0> = 0001	**N/A**	**N/A**	**N/A**	V	Reserved
			LVDL<3:0> = 0010	**2.08**	**2.26**	**2.44**	V	
			LVDL<3:0> = 0011	**2.26**	**2.45**	**2.65**	V	
			LVDL<3:0> = 0100	**2.35**	**2.55**	**2.76**	V	
			LVDL<3:0> = 0101	**2.55**	**2.77**	**2.99**	V	
			LVDL<3:0> = 0110	**2.64**	**2.87**	**3.10**	V	
			LVDL<3:0> = 0111	**2.82**	**3.07**	**3.31**	V	
			LVDL<3:0> = 1000	**3.09**	**3.36**	**3.63**	V	
			LVDL<3:0> = 1001	**3.29**	**3.57**	**3.86**	V	
			LVDL<3:0> = 1010	**3.38**	**3.67**	**3.96**	V	
			LVDL<3:0> = 1011	**3.56**	**3.87**	**4.18**	V	
			LVDL<3:0> = 1100	**3.75**	**4.07**	**4.40**	V	
			LVDL<3:0> = 1101	**3.93**	**4.28**	**4.62**	V	
			LVDL<3:0> = 1110	**4.23**	**4.60**	**4.96**	V	
D420B		LVD Voltage on V_{DD} Transition High-to-Low		Industrial **(-40°C to +85°C)**				
		PIC18F2X20/4X20	LVDL<3:0> = 1011	**3.56**	**3.87**	**4.18**	V	
			LVDL<3:0> = 1100	**3.75**	**4.07**	**4.40**	V	
			LVDL<3:0> = 1101	**3.93**	**4.28**	**4.62**	V	
			LVDL<3:0> = 1110	**4.23**	**4.60**	**4.96**	V	
D420C		LVD Voltage on V_{DD} Transition High-to-Low		Extended **(-40°C to +125°C)**				
		PIC18F2X20/4X20	LVDL<3:0> = 1011	**3.41**	**3.87**	**4.33**	V	
			LVDL<3:0> = 1100	**3.58**	**4.07**	**4.56**	V	
			LVDL<3:0> = 1101	**3.77**	**4.28**	**4.79**	V	
			LVDL<3:0> = 1110	**4.04**	**4.60**	**5.15**	V	

Legend: Shading of rows is to assist in readability of the table.

† Production tested at T_{AMB} = 25°C. Specifications over temperature limits ensured by characterization.

TABLE 26-4: LOW-VOLTAGE DETECT CHARACTERISTICS (CONTINUED)

PIC18LF2220/2320/4220/4320 (Industrial)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2220/2320/4220/4320 (Industrial, Extended)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
Date Codes from 0417xxx and higher								
D420D	VLVD	LVD Voltage on VDD Transition High-to-Low		Industrial Low Voltage **(-10°C to +85°C)**				
		PIC18LF2X20/4X20	LVDL<3:0> = 0000	**N/A**	**N/A**	**N/A**	V	Reserved
			LVDL<3:0> = 0001	**N/A**	**N/A**	**N/A**	V	Reserved
			LVDL<3:0> = 0010	**2.08**	**2.26**	**2.44**	V	
			LVDL<3:0> = 0011	**2.26**	**2.45**	**2.65**	V	
			LVDL<3:0> = 0100	**2.35**	**2.55**	**2.76**	V	
			LVDL<3:0> = 0101	**2.55**	**2.77**	**2.99**	V	
			LVDL<3:0> = 0110	**2.64**	**2.87**	**3.10**	V	
			LVDL<3:0> = 0111	**2.82**	**3.07**	**3.31**	V	
			LVDL<3:0> = 1000	**3.09**	**3.36**	**3.63**	V	
			LVDL<3:0> = 1001	**3.29**	**3.57**	**3.86**	V	
			LVDL<3:0> = 1010	**3.38**	**3.67**	**3.96**	V	
			LVDL<3:0> = 1011	**3.56**	**3.87**	**4.18**	V	
			LVDL<3:0> = 1100	**3.75**	**4.07**	**4.40**	V	
			LVDL<3:0> = 1101	**3.93**	**4.28**	**4.62**	V	
			LVDL<3:0> = 1110	**4.23**	**4.60**	**4.96**	V	
D420F		LVD Voltage on VDD Transition High-to-Low		Industrial Low Voltage **(-40°C to -10°C)**				
		PIC18LF2X20/4X20	LVDL<3:0> = 0000	**N/A**	**N/A**	**N/A**	V	Reserved
			LVDL<3:0> = 0001	**N/A**	**N/A**	**N/A**	V	Reserved
			LVDL<3:0> = 0010	**1.99**	**2.26**	**2.53**	V	
			LVDL<3:0> = 0011	**2.16**	**2.45**	**2.75**	V	
			LVDL<3:0> = 0100	**2.25**	**2.55**	**2.86**	V	
			LVDL<3:0> = 0101	**2.43**	**2.77**	**3.10**	V	
			LVDL<3:0> = 0110	**2.53**	**2.87**	**3.21**	V	
			LVDL<3:0> = 0111	**2.70**	**3.07**	**3.43**	V	
			LVDL<3:0> = 1000	**2.96**	**3.36**	**3.77**	V	
			LVDL<3:0> = 1001	**3.14**	**3.57**	**4.00**	V	
			LVDL<3:0> = 1010	**3.23**	**3.67**	**4.11**	V	
			LVDL<3:0> = 1011	**3.41**	**3.87**	**4.34**	V	
			LVDL<3:0> = 1100	**3.58**	**4.07**	**4.56**	V	
			LVDL<3:0> = 1101	**3.76**	**4.28**	**4.79**	V	
			LVDL<3:0> = 1110	**4.04**	**4.60**	**5.15**	V	

Legend: Shading of rows is to assist in readability of the table.

† Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

TABLE 26-4: LOW-VOLTAGE DETECT CHARACTERISTICS (CONTINUED)

PIC18LF2220/2320/4220/4320 (Industrial)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2220/2320/4220/4320 (Industrial, Extended)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
Date Codes from 0417xxx and higher								
D420G	VLVD	LVD Voltage on VDD Transition High-to-Low		Industrial **(-10°C to +85°C)**				
		PIC18F2X20/4X20	LVDL<3:0> = 1101	**3.93**	**4.28**	**4.62**	V	
			LVDL<3:0> = 1110	**4.23**	**4.60**	**4.96**	V	
D420H		LVD Voltage on VDD Transition High-to-Low		Industrial **(-40°C to -10°C)**				
		PIC18F2X20/4X20	LVDL<3:0> = 1101	**3.76**	**4.28**	**4.79**	V	Reserved
			LVDL<3:0> = 1110	**4.04**	**4.60**	**5.15**	V	
D420J		LVD Voltage on VDD Transition High-to-Low		Extended **(-10°C to +85°C)**				
		PIC18F2X20/4X20	LVDL<3:0> = 1101	**3.94**	**4.28**	**4.62**	V	
			LVDL<3:0> = 1110	**4.23**	**4.60**	**4.96**	V	
D420K		LVD Voltage on VDD Transition High-to-Low		Extended **(-40°C to -10°C, +85°C to +125°C)**				
		PIC18F2X20/4X20	LVDL<3:0> = 1101	**3.77**	**4.28**	**4.79**	V	Reserved
			LVDL<3:0> = 1110	**4.05**	**4.60**	**5.15**	V	

Legend: Shading of rows is to assist in readability of the table.

† Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

8. Module: PIC18F4220/4320 Pinout I/O Descriptions

In Table 1-3: PIC18F4220/4320 Pinout I/O Descriptions (page 18), QFN pin 28 was incorrectly identified as connected to VDD. The correct I/O description for QFN pin 28 is NC.

9. Module: Pinout I/O Descriptions

In Table 1-2: PIC18F2220/2320 Pinout I/O Descriptions (pages 11-13) and Table 1-3: PIC18F4220/4320 Pinout I/O Descriptions (pages 14-18), Note 1 and Note 2 are presented in the incorrect order. They have been corrected to read as follows:

Note 1: Alternate assignment for CCP2 when CCP2MX is cleared.

2: Default assignment for CCP2 when CCP2MX (CONFIG3H<0>) is set.

REVISION HISTORY

Rev A Document (04/2004)

First revision of this document, silicon issues 1 (Internal Oscillator Block), 2 (Core – DAW Instruction), 3 (Internal Oscillator Block), 4 (INTOSC), 5 (MSSP – All I^2C and SPI Modes), 6 (MSSP – SPI, Slave Mode), 7 (Data EEPROM) and data sheet clarification issues 1 (RE3 Pin), 2 (Timer1 Oscillator), 3 (Enhanced PWM Module Block Diagram), 4 (Enabling SPI I/O), 5 (DC Characteristics), 6 (DC Characteristics) and 7 (LVD Characteristics).

Rev B Document (02/2005)

Added Data Sheet Clarification issue 8 (PIC18F4220/4320 Pinout I/O Descriptions).

Rev C Document (03/2005)

Added Data Sheet Clarification issue 9 (Pinout I/O Descriptions).

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