

**MICROCHIP****PIC18F87J50 FAMILY****PIC18F87J50 Family Data Sheet Errata****Clarifications/Corrections to the Data Sheet:**

In the Device Data Sheet (DS39775B), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F87J50 family will be reported in a separate silicon errata. Please check the Microchip website ([www.microchip.com](http://www.microchip.com)) for any existing issues.

**1. Module: Table 28-1: Memory Programming Requirements**

On page 430, parameter, D132B, is renamed, and the minimum and maximum voltage levels and conditions column of the Self-Timed Erase or Write for VDD and VDDCORE for are included. The TWE parameter number and conditions column are changed. The changed content are indicated in bold text in the following table:

**TABLE 28-1: MEMORY PROGRAMMING REQUIREMENTS**

<b>DC CHARACTERISTICS</b>			<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
<b>Param No.</b>	<b>Sym</b>	<b>Characteristic</b>	<b>Min</b>	<b>Typ†</b>	<b>Max</b>	<b>Units</b>	<b>Conditions</b>
<b>Program Flash Memory</b>							
D130	EP	Cell Endurance	10K	—	—	E/W	-40°C to +85°C V <sub>MIN</sub> = Minimum operating voltage
D131	VPR	VDDCORE for Read	V <sub>MIN</sub>	—	3.6	V	
<b>D132</b>	VPEW	<b>Voltage for Self-Timed Erase or Write</b>					<b>ENVREG tied to VDD</b> <b>ENVREG tied to Vss</b>
		VDD	<b>2.35</b>	—	<b>3.6</b>	V	
		VDDCORE	<b>2.25</b>	—	<b>2.7</b>	V	
D133A	TIW	Self-Timed Write Cycle Time	—	2.8	—	ms	Provided no other specifications are violated
D133B	TIE	Self-Timed Page Erase Cycle Time	—	33.0	—	ms	
D134	TRETD	Characteristic Retention	20	—	—	Year	
D135	IDDP	Supply Current during Programming	—	10	—	mA	
<b>D140</b>	TWE	Writes per Erase Cycle	—	—	1	—	<b>For each physical address</b>

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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## 2. Module: Table 28-2: Comparator Specifications

On page 431, the maximum Input Offset Voltage (Param No. D300) is changed to  $\pm 25$  mV.

The parameter numbers for TRESP and TMC2OV are changed to D303 and D304, respectively.

A new parameter number, D305, for VIRV is added. The changed/append content are indicated in bold text in the following table:

**TABLE 28-2: COMPARATOR SPECIFICATIONS**

Operating Conditions: $3.0\text{V} < V_{DD} < 3.6\text{V}$ , $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ (unless otherwise stated)							
Param No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
D300	VIOFF	Input Offset Voltage	—	$\pm 5.0$	$\pm 25$	mV	
D301	VICM	Input Common Mode Voltage	0	—	$AV_{DD} - 1.5$	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
<b>D303</b>	TRESP	Response Time <sup>(1)</sup>	—	150	400	ns	
<b>D304</b>	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	$\mu\text{s}$	
<b>D305</b>	<b>VIRV</b>	<b>Internal Reference Voltage</b>	—	<b>1.2</b>	—	<b>V</b>	

**Note 1:** Response time measured with one comparator input at  $(V_{DD} - 1.5)/2$ , while the other input transitions from VSS to VDD.

## 3. Module: Table 28-4: Internal Voltage Regulator Specifications

On page 431, the comment for the External Filter Capacitor value, CEFC, is changed. The Minimum value of VRGOUT is removed. The note stating “\* These parameters are characterized but not tested. Parameter numbers are not yet assigned for these specifications.” is removed. The changed/append content is indicated in bold text in the following table:

**TABLE 28-4: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS**

Operating Conditions: $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ (unless otherwise stated)							
Param No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
	VRGOUT	Regulator Output Voltage*	—	2.5	—	V	$V_{DD}$ , ENVREG = 3.0V
	CEFC	External Filter Capacitor Value*	4.7	10	—	$\mu\text{F}$	<b>Capacitor must be low series resistance (&lt;5 Ohms)</b>

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## 4. Module: Section 28.3 “DC Characteristics: PIC18F87J50 family (Industrial)”

On page 428, the characteristics and conditions of the Input Leakage Current are updated for the Analog (D060) and included for the Digital (D060A) I/O ports. The changed content are indicated in bold text in the following table:

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D030 D030A D031 D032 D033 D033A D034	V <sub>IL</sub>	<b>Input Low Voltage</b> All I/O ports:				
		with TTL buffer	V <sub>SS</sub>	0.15 V <sub>DD</sub>	V	V <sub>DD</sub> < 3.3V
			—	0.8	V	3.3V ≤ V <sub>DD</sub> ≤ 3.6V
		with Schmitt Trigger buffer	V <sub>SS</sub>	0.2 V <sub>DD</sub>	V	
		$\overline{\text{MCLR}}$	V <sub>SS</sub>	0.2 V <sub>DD</sub>	V	
		OSC1	V <sub>SS</sub>	0.3 V <sub>DD</sub>	V	HS, HSPLL modes
		OSC1	V <sub>SS</sub>	0.2 V <sub>DD</sub>	V	EC, ECPLL modes
		T1CKI	V <sub>SS</sub>	0.3	V	
D040 D040A D041  Dxxx DxxxA Dxxx D042 D043 D043A D044	V <sub>IH</sub>	<b>Input High Voltage</b> I/O ports with analog functions:				
		with TTL buffer	0.25 V <sub>DD</sub> + 0.8V	V <sub>DD</sub>	V	V <sub>DD</sub> < 3.3V
			2.0	V <sub>DD</sub>	V	3.3V ≤ V <sub>DD</sub> ≤ 3.6V
		with Schmitt Trigger buffer	0.8 V <sub>DD</sub>	V <sub>DD</sub>	V	
		Digital-only I/O ports:				
		with TTL buffer	0.25 V <sub>DD</sub> + 0.8V	5.5	V	V <sub>DD</sub> < 3.3V
			2.0	5.5	V	3.3V ≤ V <sub>DD</sub> ≤ 3.6V
		with Schmitt Trigger buffer	0.8 V <sub>DD</sub>	5.5	V	
		$\overline{\text{MCLR}}$	0.8 V <sub>DD</sub>	V <sub>DD</sub>	V	
		OSC1	0.7 V <sub>DD</sub>	V <sub>DD</sub>	V	HS, HSPLL modes
		OSC1	0.8 V <sub>DD</sub>	V <sub>DD</sub>	V	EC, ECPLL modes
		T1CKI	1.6	V <sub>DD</sub>	V	
D060  <b>D060A</b>  D061 D063	I <sub>IL</sub>	<b>Input Leakage Current<sup>(1)</sup></b> I/O ports with Analog functions	—	±1	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , Pin at high-impedance
		Digital only I/O ports	—	±1	μA	<b>V<sub>SS</sub> ≤ V<sub>PIN</sub> ≤ 5.5V,</b> <b>Pin at high-impedance</b>
		$\overline{\text{MCLR}}$	—	±1	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub>
		OSC1	—	±5	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub>

**Note 1:** Negative current is defined as current sourced by the pin.

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## 5. Module: Section 19.3 “SPI Mode” and Section 19.4 “I<sup>2</sup>C™ Mode”

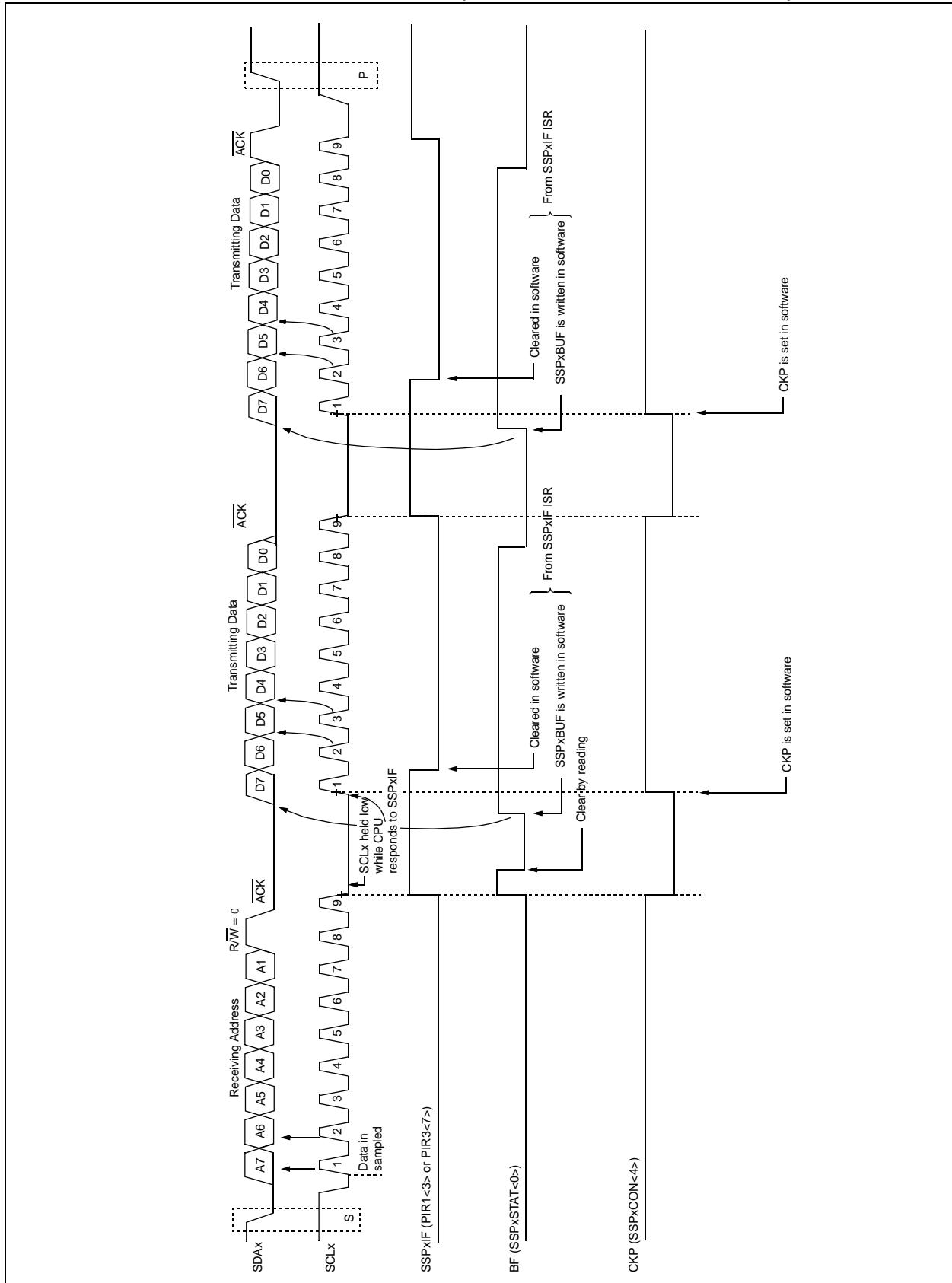
In **Section 19.3 “SPI Mode”** on page 231 and **Section 19.4 “I<sup>2</sup>C™ Mode”** on page 241, the following new note is included to describe the procedure to disable the MSSP module:

<p><b>Note:</b> Disabling the MSSP module by clearing the SSPEN (SSPxCON1&lt;5&gt;) bit may not reset the module. It is recommended to clear the SSPxSTAT, SSPxCON1 and SSPxCON2 registers and select the mode prior to setting the SSPEN bit to enable the MSSP module.</p>
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## 6. Module: Figure 19-10: I<sup>2</sup>C™ Slave Mode Timing (Transmission, 7-Bit Address)

On page 252, the figure is replaced with the new timing diagram provided in Figure 19-10.

**FIGURE 19-10: I<sup>2</sup>C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)**



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## 7. Module: **Figure 19-24: I<sup>2</sup>C™ Master Mode Waveform (Reception, 7-Bit Address)**

On page 269, the condition (R/ $\overline{W}$ ) when the Acknowledge signal (ACK) is received from the slave, after transmitting the address to the slave, is changed to '1'. The changed value is indicated in bold text in Figure 19-24.



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## REVISION HISTORY

### Rev A Document (10/2008)

Initial release of this document. Includes Data Sheet Clarification issues 1 (Table 28-1: Memory Programming Requirements), 2 (Table 28-2: Comparator Specifications), 3 (Table 28-4: Internal Voltage Regulator Specifications), 4 (Section 28.3 "DC Characteristics: PIC18F87J50 Family (Industrial)"), 5 (Section 19.3 "SPI Mode" and Section 19.4 "I<sup>2</sup>C™ Mode"), 6 (Figure 19-10: I<sup>2</sup>C™ Slave Mode Timing – Transmission, 7-Bit Address) and 7 (Figure 19-24: I<sup>2</sup>C™ Master Mode Waveform – Reception, 7-Bit Address).



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