

**MICROCHIP****PIC18F6627/6722/8627/8722****PIC18F6627/6722/8627/8722 Rev. B1 Silicon Errata**

The PIC18F6627/6722/8627/8722 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS39646B), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6627/6722/8627/8722 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F6627/6722/8627/8722 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6627	0001 0011 110	0 0010
PIC18F6722	0001 0100 000	0 0010
PIC18F8627	0001 0011 111	0 0010
PIC18F8722	0001 0100 001	0 0010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFEh:3FFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F6627/6722/8627/8722 silicon.

1. Module: Master Synchronous Serial Port (MSSP) — Serial Peripheral Interface (SPI)

In SPI mode, the Buffer Full flag (BF bit in the SSPxSTAT register), the Write Collision Detect bit (WCOL in SSPxCON1) and the Receive Overflow Indicator bit (SSPOV in SSPxCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPxCON1 register).

For example, if SSPxBUF is full (BF bit is set), and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPxBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

Ensure that if the buffer is full, SSPxBUF is read (thus clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Capture/Compare/PWM (CCP)

PWM output of 10-bit resolution is not available for either CCP4 or CCP5 when Timer4 is being used as the PWM time base (T3CON<6,3> = 01, 10 or 11) for the PWM mode (CCPxCON<3:2> = 11).

Work around

For 10-bit resolution, use Timer2 as the PWM time base (T3CON<6,3> = 00).

For 8-bit resolution, use Timer4 or Timer2 as the PWM time base and set the two LSBs to '00' (CCPxCON<5:4> = 00).

Date Codes that pertain to this issue:

All engineering and production devices.

PIC18F6627/6722/8627/8722

REVISION HISTORY

Rev A Document (8/2007)

Initial release of this errata. Includes silicon issues
1 (MSSP) and 2 (CCP).

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