PIC18F85J11 FAMILY

PIC18F85J11 Family Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39774**C**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F85J11 family will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Section 10.1.1 "Input Pins and Voltage Considerations"

Section 10.1.1 "Input Pins and Voltage Considerations", on page 123, is changed. The changed content is indicated in bold text in the following paragraph:

The voltage tolerance of pins used as device inputs is dependent on the pin's input function. **Most** pins that are used as digital only inputs are able to handle DC voltages up to 5.5V, a level typical for digital logic circuits. **The digital pins that cannot exceed VDD are RE0, RE1, RE2, RG0, RG2 and RG3**.

In contrast, pins that also have analog input functions of any kind can only tolerate voltages up to VDD. Voltage excursions beyond VDD on these pins should be avoided.

Table 10-1 summarizes the input voltage capabilities. Refer to **Section 25.0 "Electrical Characteristics"** for more details.

TABLE 10-1: Input Voltage Tolerance

Port or Pin	Tolerated Input	Description
PORTA<7:5>	VDD	Only VDD input levels tolerated.
PORTA<3:0>		
PORTC<1:0>		
PORTE<2:0>		
PORTF<7:1>		
PORTG<3:2>		
PORTG<0>		
PORTA<4>	5.5V	Tolerates input levels above VDD, useful for most standard logic.
PORTB<7:0>		
PORTC<7:2>		
PORTD<7:0>		
PORTE<7:3>		
PORTG<4>		
PORTG<1>		
PORTH<7:0>(1)		
PORTJ<7:0>(1)		

Note 1: Not available on 64-pin devices.

2. Module: PORTD, TRISD and LATD Registers

On the third paragraph of **Section 10.5 "PORTD, TRISD and LATD Registers"** on page 131, the description to disable the pull-ups is changed. The changed content is indicated in bold text in the following paragraph:

Each of the PORTD pins has a weak internal pull-up. A single control bit can turn off all the pull-ups. This is performed by **clearing** bit RDPU (PORTG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on all device Resets.

3. Module: Register 17-3: BAUDCON1: Baud Rate Control Register 1

On page 220, bit 6 and bit 4 are renamed and bit 5 is changed. The changed content is indicated in bold text in Register 17-3:

REGISTER 17-3: BAUDCON1: BAUD RATE CONTROL REGISTER 1

R/W-0	R-1	**R/W-0**	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is active

bit 5 **RXDTP**: **Data/Receive Polarity Select bit**
Asynchronous mode:
1 = Receive data (RXx) is inverted (active-low)
0 = Receive data (RXx) is not inverted (active-high)
Synchronous mode:
1 = Data (DTx) is inverted (active-low)
0 = Data (DTx) is not inverted (active-high)

bit 4 **TXCKP**: Synchronous Clock Polarity Select bit
Asynchronous mode:
1 = Idle state for transmit (TXx) is a low level
0 = Idle state for transmit (TXx) is a high level
Synchronous mode:
1 = Idle state for clock (CKx) is a high level
0 = Idle state for clock (CKx) is a low level

bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH1 and SPBRG1
0 = 8-bit Baud Rate Generator – SPBRG1 only (Compatible mode), SPBRGH1 value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RX1 pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge
0 = RX1 pin not monitored or rising edge detected
Synchronous mode:
Unused in this mode.

REGISTER 17-3: BAUDCON1: BAUD RATE CONTROL REGISTER 1 (CONTINUED)

bit 0 **ABDEN**: Auto-Baud Detect Enable bit

Asynchronous mode:

1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.

0 = Baud rate measurement disabled or completed

Synchronous mode:

Unused in this mode.

4. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

Bits 6, 5 and 4 are renamed In the following tables:

- Table 17-2: Registers Associated with the Baud Rate Generator (on page 221)
- Table 17-5: Registers Associated with Asynchronous Transmission (on page 227)
- Table 17-6: Registers Associated with Asynchronous Reception (on page 229)

The changed content is indicated in bold text in the following tables:

TABLE 17-2: REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	54
SPBRGH1	EUSART Baud Rate Generator Register High Byte								54
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the BRG.

TABLE 17-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	53
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	53
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	53
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
TXREG1	EUSART Transmit Register								53
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	**ABDEN**	54
SPBRGH1	EUSART Baud Rate Generator Register High Byte								54
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53
LATG	U2OD	U1OD	—	LATG4	LATG3	LATG2	LATG1	LATG0	54

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

TABLE 17-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	53
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	53
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	53
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
RCREG1	EUSART Receive Register								53
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	54
SPBRGH1	EUSART Baud Rate Generator Register High Byte								54
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

5. Module: Table 4-2: Initialization Conditions for all Registers

On page 51, the values for the Resets and WDT wake-up and interrupt are changed. The changed content is indicated in bold text in Table 4-2.

TABLE 4-2: Initialization Conditions For All Registers

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
...					
SPBRGH1	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu
BAUDCON1	PIC18F6XJ11	PIC18F8XJ11	**0100 0-00**	**0100 0-00**	**uuuu u-uu**
CCPR1H	PIC18F6XJ11	PIC18F8XJ11	xxxx xxxx	uuuu uuuu	uuuu uuuu
...					

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 4-1 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read as '0'.

6. Module: Table 5-4: PIC18F85J11 Family Register File Summary

On page 73, bit 2 and the POR/BOR values are changed for register, PORTE. On page 74, bits 6, 5 and 4 are renamed and the POR/BOR values are changed for registers, BAUDCON1, SPBRGH1 and CCPR1H.

The changed content is indicated in bold text in Table 5-4.

TABLE 5-4: PIC18F85J11 FAMILY Register File Summary

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page
...										
SPBRGH1	EUSART Baud Rate Generator High Byte								0000 0000	54, 221
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	**0100 0-00**	54, 220
CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	54, 164
...										
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	—	xxxx xxx-	54, 138
PORTE	RE7	RE6	RE5	RE4	RE3	**RE2**	RE1	RE0	**xxxx xxxx**	54, 136
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	54, 133
...										

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved, do not modify

Note 1: Bit 21 of the PC is only available in Test mode and Serial Programming modes.

2: These registers and/or bits are available only on 80-pin devices; otherwise, they are unimplemented and read as '0'. Reset states shown are for 80-pin devices.

3: Alternate names and definitions for these bits when the MSSP module is operating in I^2C™ Slave mode. See Section 16.4.3.2 "Address Masking" for details.

4: The PLLEN bit is only available in specific oscillator configurations; otherwise, it is disabled and reads as '0'. See Section 2.4.3 "PLL Frequency Multiplier" for details.

5: RA6/RA7 and their associated latch and direction bits are configured as port pins only when the internal oscillator is selected as the default clock source (FOSC2 Configuration bit = 0); otherwise, they are disabled and these bits read as '0'.

7. Module: Table 25-1: Memory Programming Requirements

On page 352, the values of VPEW (formerly Parameter D132B, which is now renamed to D132) are changed. Parameter number D1xx (TWE) is renamed to D140, and its conditions column is updated. Parameter D133A (TIW) is renamed to D133. The changed content is indicated in bold text in Table 25-1.

TABLE 25-1: Memory Programming Requirements

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	100K	1K	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132	VPEW	**Voltage for Self-Timed Erase or Write**					
		VDD	**2.35**	**—**	**3.6**	**V**	**ENVREG tied to VDD**
		VDDCORE	**2.25**	**—**	**2.7**	**V**	**ENVREG tied to VSS**
D133	TIW	Self-Timed Write Cycle Time	—	2.8	—	ms	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided, no other specifications are violated
D135	IDDP	Supply Current during Programming	—	3	7	mA	—
D1**40**	TWE	Writes per Erase Cycle	—	—	1	—	**For each physical address**

† Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

8. Module: Table 25-2: Comparator Specifications

On page 353, the maximum Input Offset Voltage (Param No. D300) is changed from ±10 mV to ±25 mV. The parameter numbers for TRESP and TMC2OV are changed to D303 and D304, respectively. Parameter D305 for VIRV is added. The note stating "*** These parameters are characterized but not tested.**" is removed. The modified values are indicated in bold text in the following table.

TABLE 25-2: Comparator Specifications

Operating Conditions: 3.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	± 5.0	± **25**	mV	—
D301	VICM	Input Common Mode Voltage	0	—	AVDD – 1.5	V	—
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	—
D303	TRESP	Response Time(1)	—	150	400	ns	—
D304	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	µs	—
D305	**VIRV**	**Internal Reference Voltage**	**—**	**1.2**	**—**	**V**	**—**

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

9. Module: Table 25-4: Internal Voltage Regulator Specifications

On page 353, the comments for the External Filter Capacitor value, CEFC, are changed. The modified value is indicated in bold text in the following table:

TABLE 25-4: Internal Voltage Regulator Specifications

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	VRGOUT	Regulator Output Voltage	—	2.5	—	V	—
	CEFC	External Filter Capacitor Value	4.7	10	—	µF	**Capacitor must be low series resistance (<5 Ohms)**

10. Module: Section 16.3 “SPI Mode” and Section 16.4 “I²C™ Mode”

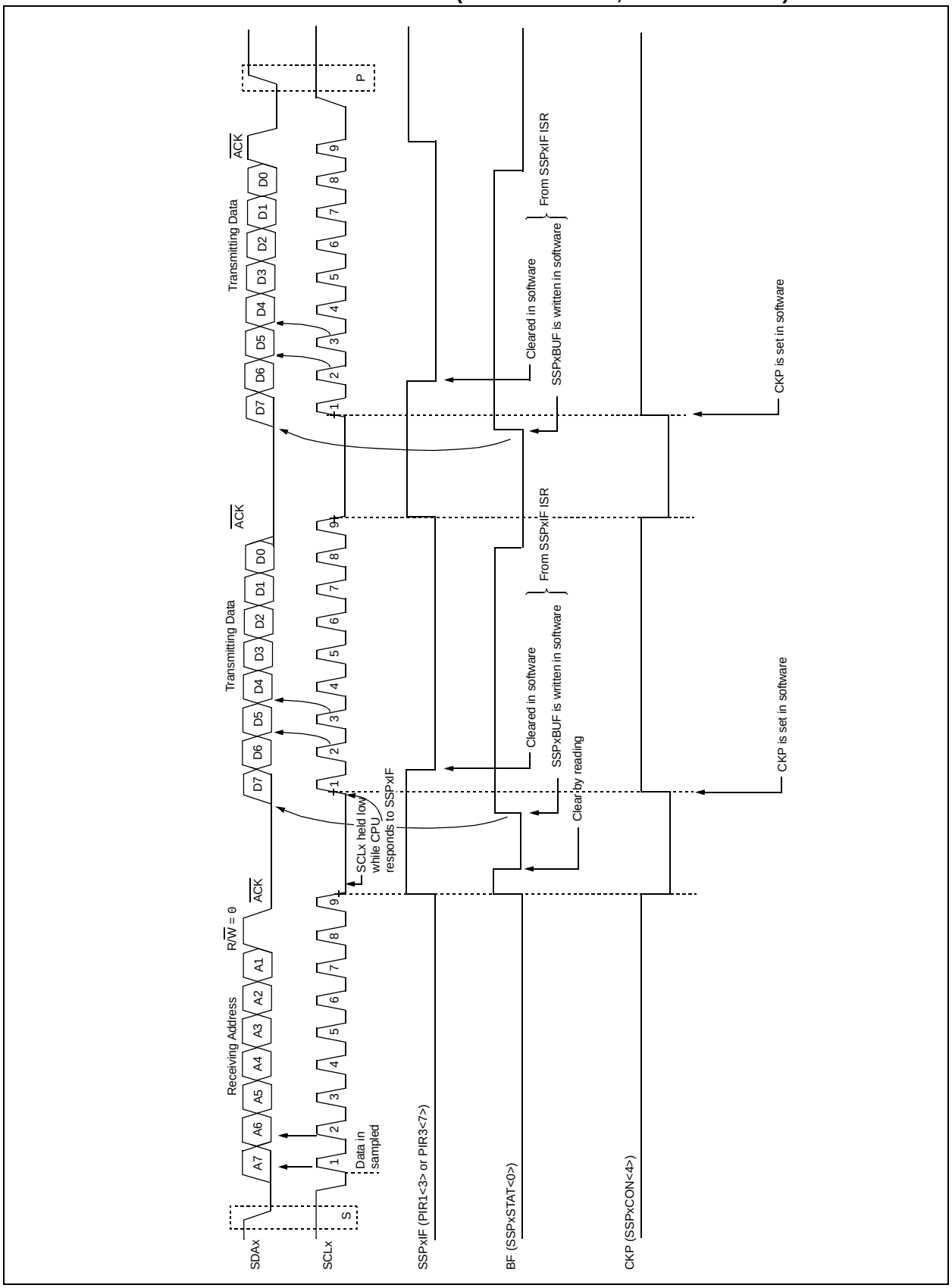
In **Section 16.3 “SPI Mode”** on page 173 and **Section 16.4 “I²C™ Mode”** on page 182, the following new note is included to describe the necessary procedure to disable the MSSP module:

Note:	Disabling the MSSP module by clearing the SSPEN (SSPCON1<5>) bit may not reset the module. It is recommended to clear the SSPSTAT, SSPCON1 and SSPCON2 registers and select the mode prior to setting the SSPEN bit to enable the MSSP module.

11. Module: Figure 16-10: I²C™ Slave Mode Timing (Transmission, 7-Bit Address)

On page 192, the figure is replaced with the new timing diagram provided in Figure 16-10.

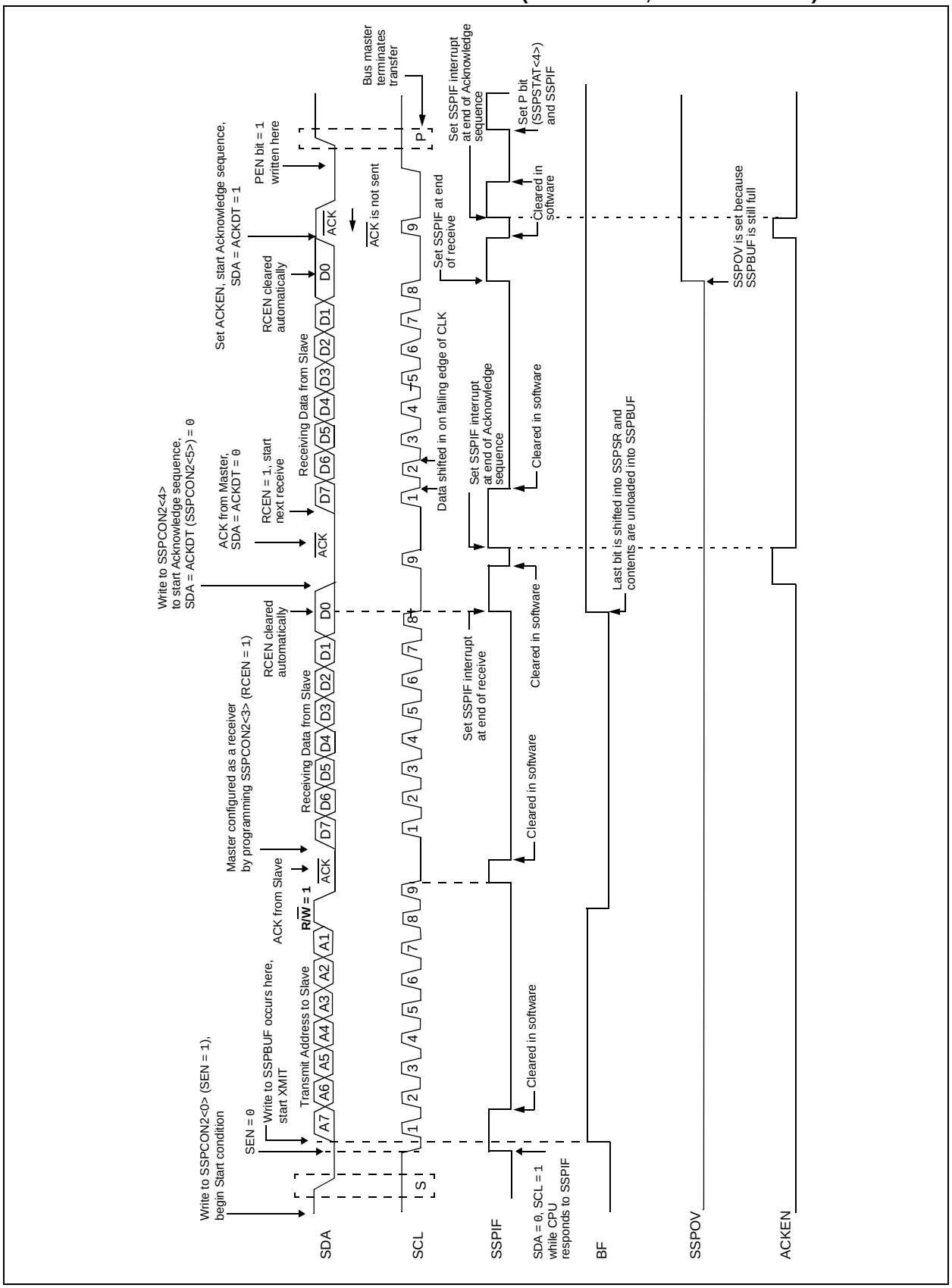
FIGURE 16-10: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)



12. Module: Figure 16-24: I²C™ Master Mode Waveform (Reception, 7-Bit Address)

On page 209, the condition (R/$\overline{W}$) when the Acknowledge signal (ACK) is received from the slave, after transmitting the address to the slave, is changed to '1'. The changed value is indicated in bold text in Figure 16-24.

FIGURE 16-24: I²C™ MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



13. Module: Section 25-3 "DC Characteristics: PIC18F85J11 Family (Industrial)"

On page 350, the Input Leakage Current is changed. The Analog (D060) has been edited and a new parameter has been added to the Digital (D060A) I/O ports. The changed values are indicated in bold text in the following table.

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		All I/O ports:				
D030		with TTL buffer	VSS	0.15 VDD	V	
D031		with Schmitt Trigger buffer	VSS	0.2 VDD	V	
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		OSC1	VSS	0.3 VDD	V	HS, HSPLL modes
D033A		OSC1	VSS	0.2 VDD	V	EC, ECPLL modes(1)
D034		T13CKI	VSS	0.3	V	
	VIH	**Input High Voltage**				
		I/O ports with 5.5V tolerance:(2)				
D040		with TTL buffer	0.25 VDD + 0.8V	VDD	V	VDD < 3.3V
D041		with Schmitt Trigger buffer	0.8 VDD	VDD	V	
		I/O ports with non 5.5V tolerance:(2)				
Dxxx		with TTL buffer	0.25 VDD + 0.8V	5.5	V	VDD < 3.3V
DxxxA			2.0	5.5	V	3.3V ≤ VDD ≤ 3.6V
Dxxx		with Schmitt Trigger buffer	0.8 VDD	5.5	V	
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		OSC1	0.7 VDD	VDD	V	HS, HSPLL modes
D043A		OSC1	0.8 VDD	VDD	V	EC, ECPLL modes
D044		T13CKI	1.6	VDD	V	
	IIL	**Input Leakage Current(1)**				
D060		**I/O ports with 5.5V tolerance:(2)**	—	±1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
D060A		**I/O ports with non 5.5V tolerance:(2)**	—	±1	µA	**VSS ≤ VPIN ≤ 5.5V, pin at high-impedance**
D061		$\overline{MCLR}$	—	±1	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	±1	µA	VSS ≤ VPIN ≤ VDD
	IPU	**Weak Pull-up Current**				
D070	IPURB	PORTB weak pull-up current	30	240	µA	VDD = 3.3V, VPIN = VSS

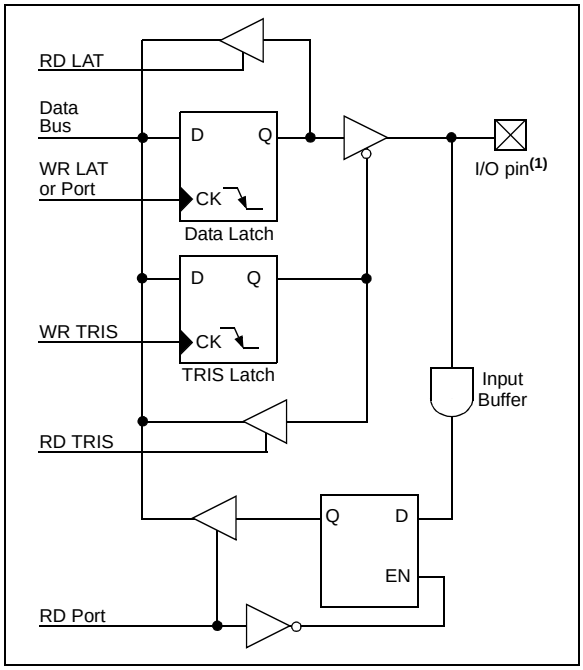
Note 1: Negative current is defined as current sourced by the pin.

2: Refer to Table 10-1 for the pins that have corresponding tolerance limits.

14. Module: Figure 9-1: Generic I/O Port Operation

The note in Figure 9-1 on page 123 is removed.

FIGURE 9-1: GENERIC I/O PORT OPERATION



15. Module: Register 9-12: IPR3

In Register 9-12, on page 120, the POR conditions for the below interrupt priority bits of the Peripheral Interrupt Priority Register 3 (IPR3) have been changed.

AUSART Receive Priority Flag Bit (RC2IP): The POR condition should be changed to R-1 instead of R-0.

AUSART Transmit Interrupt Priority Bit (TX2IP): The POR condition should be changed to R-1 instead of R-0.

The modified value is indicated in bold text in the below table.

REGISTER 9-12: IPR3: PERIPHERAL INTERRUPT PRIORITY REGISTER 3

U-0	U-0	**R-1**	**R-1**	U-0	R/W-1	R/W-1	U-0
—	—	RC2IP	TX2IP	—	CCP2IP	CCP1IP	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REVISION HISTORY

Rev A Document (7/2008)

Initial release of this errata includes Data Sheet Clarification issue 1 (Section 10.1.1 “Input Pins and Voltage Considerations”), 2 (PORTD, TRISD and LATD Registers), 3 (Register 17-3: BAUDCON1: baud Rate Control 1) and 4 (Enhanced Universal Synchronous Asynchronous Receiver Transmitter – EUSART).

Rev B Document (10/2008)

Added Data Sheet Clarification issues 5 (Table 4-2: Initialization Conditions for all Registers), 6 (Table 5-4: PIC18F85J11 Family Register File), 7 (Table 25:1: Memory Programming Requirements), 8 (Table 25-2: Comparator Specifications), 9 (Table 25-4: Internal Voltage Regulator Specifications), 10 (Section 16.3 “SPI Mode” and Section 16.4 “I^2C Mode”), 11 (Figure 16-10: I^2C Slave Mode Timing – Transmission, 7-Bit Address), 12 (Figure 16-24: I^2C Master Mode Waveform – Reception, 7-Bit Address), 13 (Section 25-3 “DC Characteristics: PIC18F85J11 Family – Industrial”), 14 (Figure 9-1: Generic I/O Port Operation) and 15 (Register 9-12: IPR3).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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