PIC18F45J10 Family Data Sheet Errata

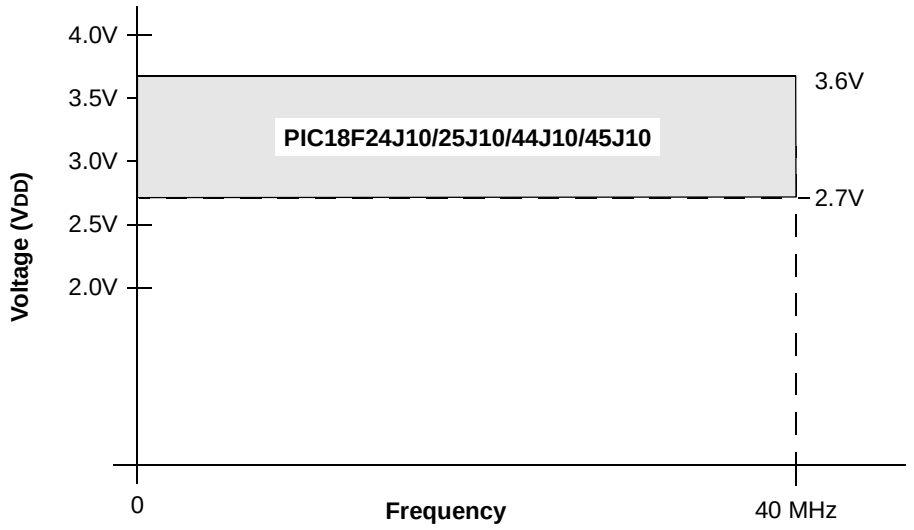
Clarifications/Corrections to the Data Sheet:

In the PIC18F45J10 Family Device Data Sheet (DS39682**C**), the following clarifications and corrections should be noted. Any silicon issues related to this device will reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Electrical Specifications (V/F Performance)

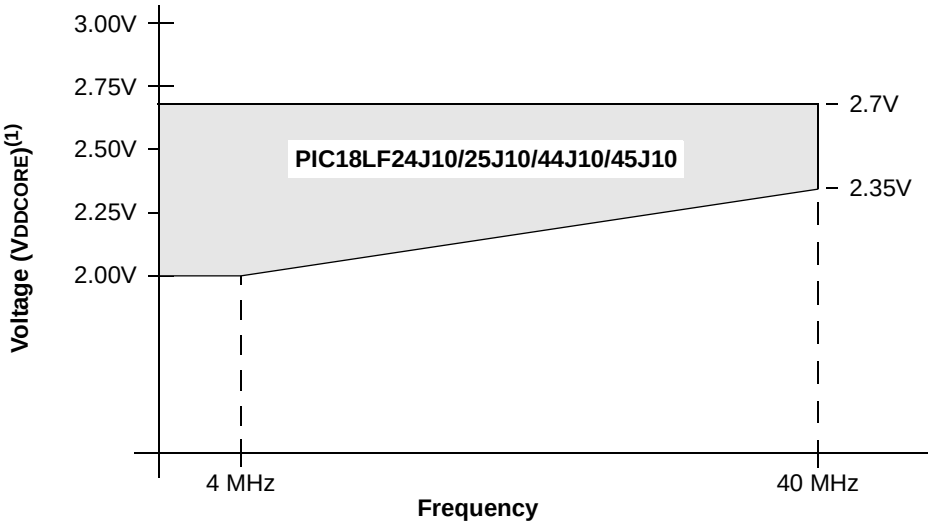
Figures 23-1 and 23-2 of the device data sheet, documenting frequency performance of the devices across the VDD range, have been updated. The new versions of the graphs are presented below.

FIGURE 23-1: PIC18F45J10 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)(1)



Note 1: For these devices, the regulator BOR circuit will automatically trigger a device Reset before VDD reaches a level at which full-speed operation is not possible.

FIGURE 23-2: PIC18LF45J10 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



For frequencies between 4 MHz and 40 MHz, FMAX = (51.42 MHz/V) * (VDDCORE – 2V) + 4 MHz

Note 1: For devices without the voltage regulator, VDD and VDDCORE must be maintained so that VDDCORE ≤ VDD ≤ 3.6V.

2. Module: Table 23-1: Memory Programming Requirements

On page 307, the parameter D132, which gives the minimum and maximum voltage levels of the Self-Timed Erase or Write for VDD and VDDCORE, has been included. Parameter D133B and D140 and their corresponding values are added. The changed/appended values are indicated in bold text in the following table:

TABLE 23-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	100	1K	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132	VPEW	**Voltage for Self-Timed Erase or Write**					
		VDD	**2.7**	—	**3.6**	V	**PIC18FXXJ10**
		VDDCORE	**2.25**	—	**2.7**	V	**PIC18LFXXJ10**
D133A	TIW	Self-Timed Write Cycle Time	—	2.8	—	ms	
D133B	TIE	**Self-Timed Page Erased Cycle Time**	**—**	**33.0**	**—**	**ms**	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided, no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	
D140	**TWE**	**Writes per Erase Cycle**	**—**	**—**	**1**	**—**	**For each physical address**

† Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3. Module: Table 23-2: Comparator Specifications

On page 308, the maximum Input Offset Voltage (Param No. D300) is changed to ±25 mV.

The parameter numbers for TRESP, TMC2OV and VIRV are changed to D303 and D304, respectively.

The parameter D305 for Internal Reference Voltage is added.

The note stating "* These parameters are characterized but not tested." is removed.

The changed content is indicated in bold text in the following table:

TABLE 23-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 3.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	± 5.0	± **25**	mV	
D301	VICM	Input Common Mode Voltage	0	—	VDD – 1.5	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
D303	TRESP	Response Time**(1)**	—	150	400	ns	
D304	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	µs	
D305	**VIRV**	**Internal Reference Voltage**	**—**	**1.2**	**—**	**V**	

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

4. Module: Table 23-4: Internal Voltage Regulator Specifications

On Page 308, the comment for the External Filter Capacitor value, CEFC, is changed. The note stating "* These parameters are characterized but not tested. Parameter numbers not yet assigned for these specifications." is removed. The modified value is indicated in bold text in the following table:

TABLE 23-4: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	VRGOUT	Regulator Output Voltage	—	2.5	—	V	—
	CEFC	External Filter Capacitor Value	4.7	10	—	µF	**Capacitor must be low series resistance (<5 Ohms)**

5. Module: Section 23.1 “DC Characteristics: Supply Voltage”

On page 297, a new parameter, D005, which which gives the voltage limits for Brown-out Reset (BOR) is added. The changed content is indicated in bold text in the following table.

23.1 DC Characteristics: Supply Voltage PIC18F24J10/25J10/44J10/45J10 (Industrial) PIC18LF24J10/25J10/44J10/45J10 (Industrial)

PIC18F45J10 Family (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	VDDCORE	—	3.6	V	PIC18LF4XJ10, PIC18LF2XJ10
D001	VDD	**Supply Voltage**	2.7(1)	—	3.6	V	PIC18F4X/2XJ10
D001B	VDDCORE	**External Supply for Microcontroller Core**	2.0	—	2.7	V	Valid only in parts designated “LF”. See **Section 20.3 “On-Chip Voltage Regulator”** for details.
D002	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	—
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	—	TBD	V	See **Section 4.3 “Power-on Reset (POR)”** for details.
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 4.3 “Power-on Reset (POR)”** for details.
D005	**VBOR**	**Brown-out Reset (BOR) Voltage**	**2.35**	**2.5**	**2.7**	**V**	

Legend: TBD = To Be Determined

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

6. Module: Section 23.3 “DC Characteristics: PIC18F45J10 Family (Industrial)

On page 305, the characteristics and conditions of the Input Leakage Current are updated for the Analog (D060) and included for the Digital (D060A) I/O ports. The changed values are indicated in bold text in the following table:

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		All I/O ports:				
D030		with TTL buffer	VSS	0.15 VDD	V	VDD < 3.3V
D030A			—	0.8	V	3.3V ≤ VDD ≤ 3.6V
D031		with Schmitt Trigger buffer	VSS	0.2 VDD	V	
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		OSC1	VSS	0.3 VDD	V	HS, HSPLL modes
D033A		OSC1	VSS	0.2 VDD	V	EC, ECPLL modes(1)
D034		T1CKI	VSS	0.3	V	
	VIH	**Input High Voltage**				
		I/O ports with 5.5V tolerance:(4)				
D040		with TTL buffer	0.25 VDD + 0.8V	VDD	V	VDD < 3.3V
D040A			2.0	VDD	V	3.3V ≤ VDD ≤ 3.6V
D041		with Schmitt Trigger buffer	0.8 VDD	VDD	V	
		I/O ports with non 5.5V tolerance:(4)				
Dxxx		with TTL buffer	0.25 VDD + 0.8V	5.5	V	VDD < 3.3V
DxxxA			2.0	5.5	V	3.3V ≤ VDD ≤ 3.6V
Dxxx		with Schmitt Trigger buffer	0.8 VDD	5.5	V	
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		OSC1	0.7 VDD	VDD	V	HS, HSPLL modes
D043A		OSC1	0.8 VDD	VDD	V	EC, ECPLL modes
D044		T1CKI	1.6	VDD	V	
	IIL	**Input Leakage Current(2,3)**				
D060		**I/O ports with 5.5V tolerance:(4)**	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		**I/O ports with non 5.5V tolerance:(4)**	**—**	**±1**	**µA**	**VSS ≤ VPIN ≤ 5.5V, Pin at high-impedance**
D061		$\overline{MCLR}$	—	±1	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	±5	µA	VSS ≤ VPIN ≤ VDD

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Refer to Table 9-2 for the pins that have corresponding tolerance limits.

7. Module: Section 15.3 “SPI Mode” and Section 15.4 “I²C™ Mode”

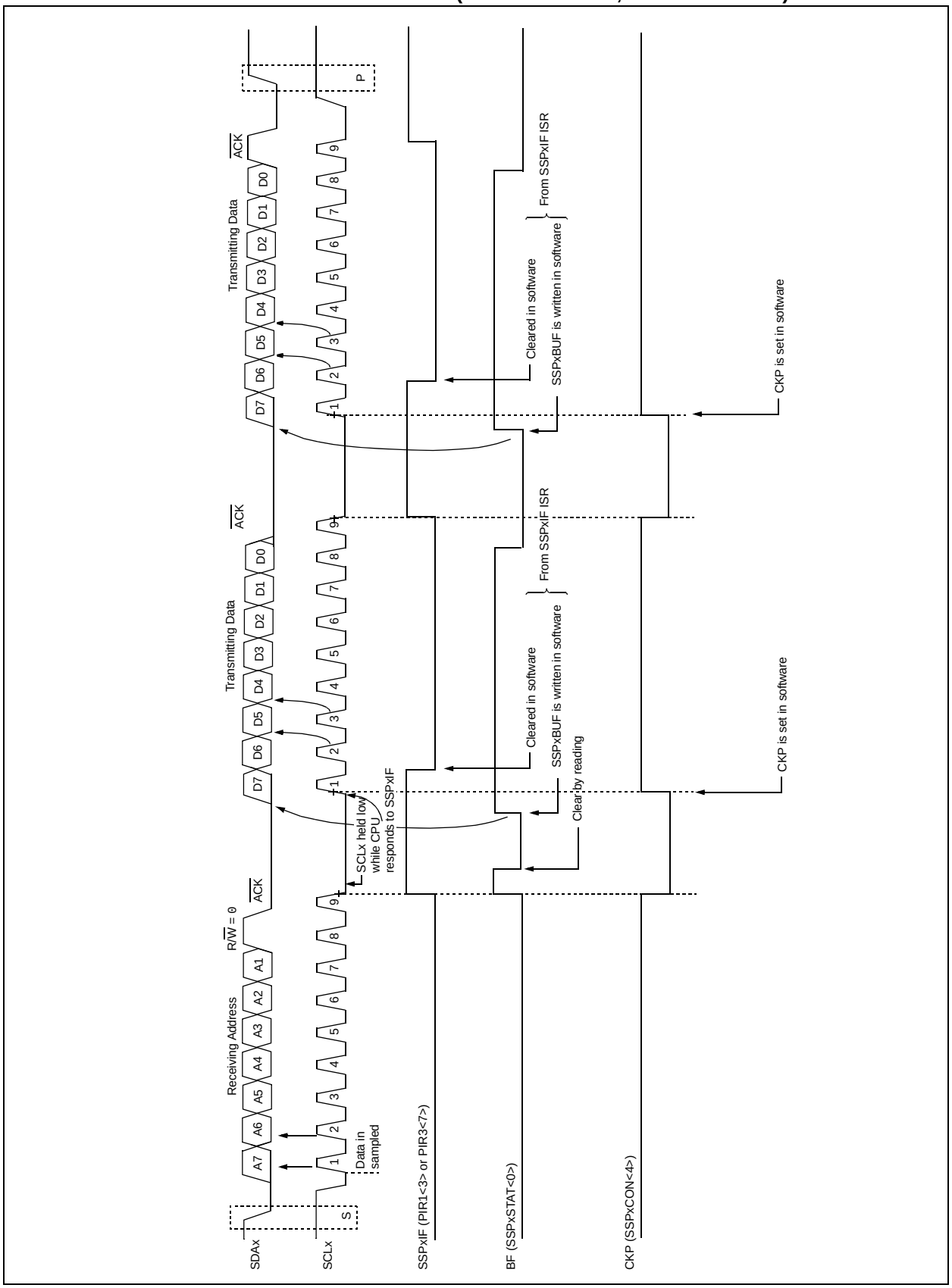
In **Section 15.3 “SPI Mode”** on page 145 and **Section 15.4 “I²C Mode”** on page 155, the following new note is included to describe the procedure to disable the MSSP module:

Note:	Disabling the MSSP module by clearing the SSPEN (SSPxCON1<5>) bit may not reset the module. It is recommended to clear the SSPxSTAT, SSPxCON1 and SSPxCON2 registers and select the mode prior to setting the SSPEN bit to enable the MSSP module.

8. Module: Figure 15-9: I²C™ Slave Mode Timing (Transmission, 7-Bit Address)

On page 162, the figure is replaced with a new timing diagram provided in Figure 15-9.

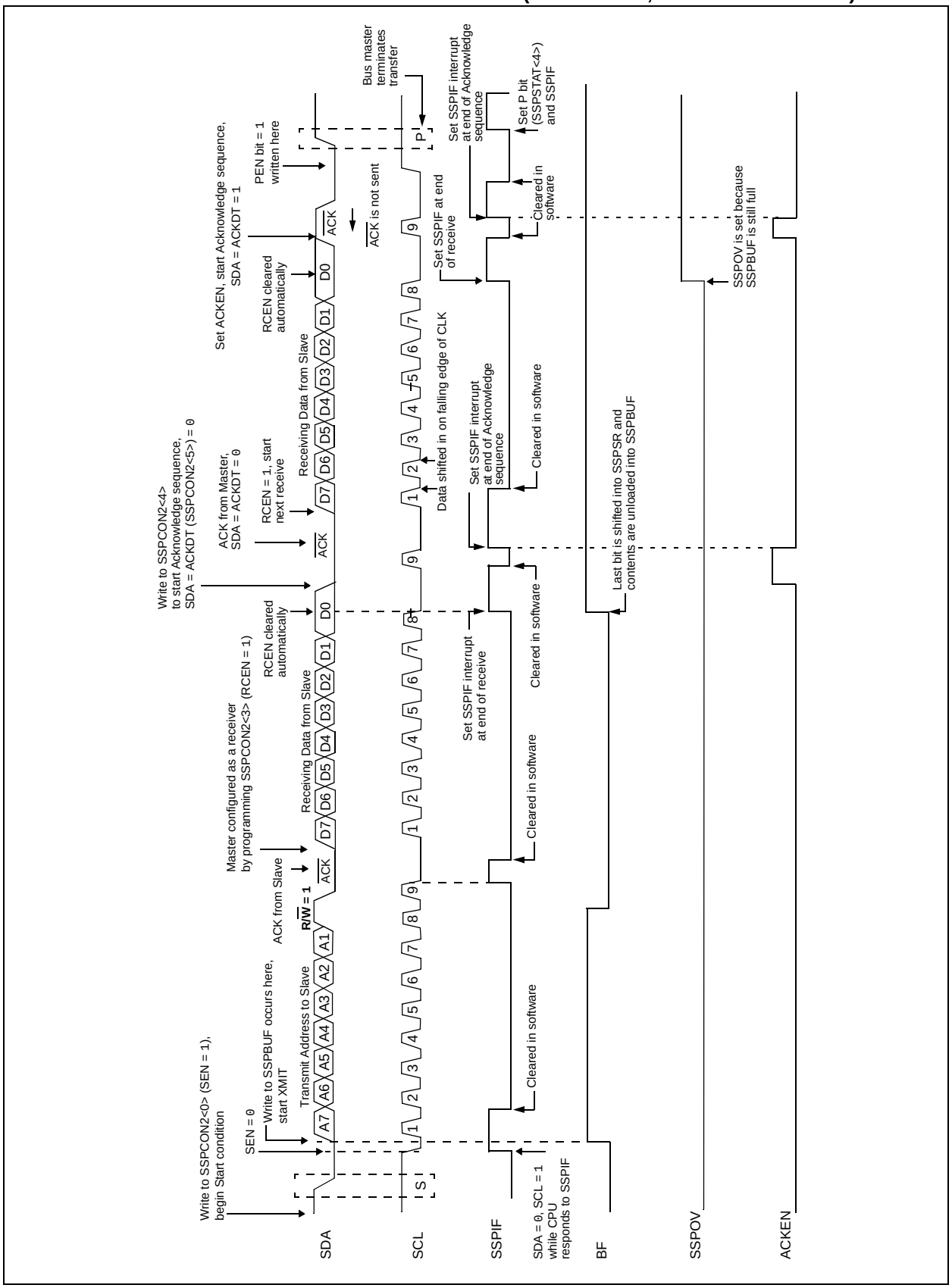
FIGURE 15-9: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)



9. Module: Figure 15-22: I²C™ Master Mode Waveform (Reception, 7-Bit Address)

On page 178, the condition (R/$\overline{W}$) when the Acknowledge signal (ACK) is received from the slave, after transmitting the address to the slave, is changed to '1'. The changed value is indicated in bold text in Figure 15-22.

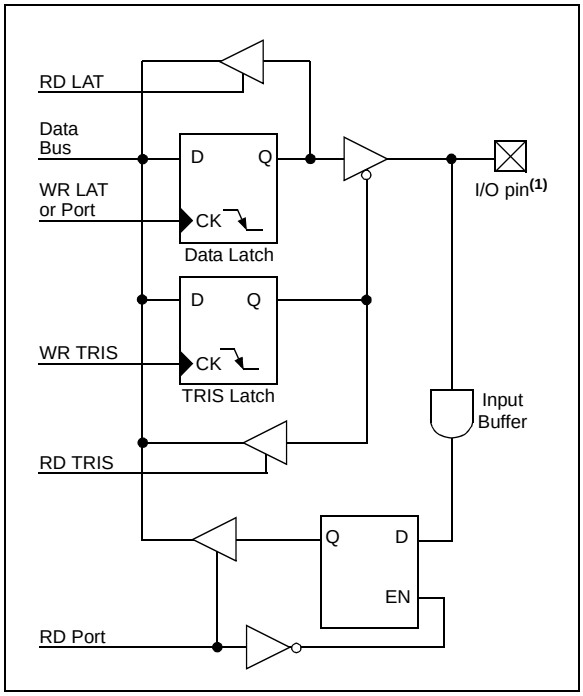
FIGURE 15-22: I²C™ MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESSING)



10. Module: Figure 9-1: Generic I/O Port Operation

The note in Figure 9-1 on page 93 is removed.

FIGURE 9-1: GENERIC I/O PORT OPERATION



REVISION HISTORY

Rev A Document (03/2006)

Original version of this document. Includes Data Sheet Clarification 1 (Electrical Specifications – V/F Performance).

Rev C Document (10/2008)

Added data sheet clarification issues 2 (Table 23-1: Memory Programming Requirements), 3 (Table 23-2: Comparator Specifications), 4 (Table 23-4: Internal Voltage Regulator Specifications), 5 (Section 23.1 “DC Characteristics”), 6 (Section 23.3 “DC Characteristics”), 7 (Section 15.3 “SPI Mode” and Section 15.4 “I^{2}C™ Mode”), 8 (Figure 15-9: I^{2}C™ Slave Mode Timing – Transmission, 7-Bit Address), 9 (Figure 15-22: I^{2}C™ Master Mode Waveform – Reception, 7-Bit Address) and 10 (Figure 9-1: Generic I/O Port Operation).

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