PIC18F24/25/44/45K20 Device IDs Rev. 0x16 and 0x18 Silicon/Data Sheet Errata

The PIC18F24/25/44/45K20 parts you have received conform functionally to the Device Data Sheet (DS41303**D**) and the Programming Specification (DS41297**D**), except for the anomalies described below.

All problems listed here will be addressed in future revisions of the PIC18F24/25/44/45K20 silicon.

1. Module: ECCP

Changing direction in Full-Bridge mode inserts a dead-band time of 4/FOSC * TMR2 Prescale instead of 1/FOSC * TMR2 Prescale as specified in the data sheet.

Work around

None.

2. Module: ECCP

ECCP – In Full-Bridge mode when PR2 = CCPR1L and DC1B[1:0] <>'00' and the direction is changed then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for TOSC * TMR2Presale * DC1B[1:0].

Work around

Avoid changing direction when the duty cycle is within three Least Significant steps of 100% duty cycle. Instead, clear the DC1B[1:0] bits before the direction change and then set them to the desired value after the direction change is complete.

3. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011) and the CKE bit of the SSPSTAT register is '1', then when SSPBUF is written, the SCK output is improperly immediately driven to the non-Idle state together with the MSb value of the SSPBUF. The duration at which SDO and SCK remain at these levels may be shorter than a full half-bit period. The remaining bits in the byte are output properly.

Work around

None.

4. Module: MSSP SPI

In SPI Master mode, when the CKE bit of the SSPSTAT register is cleared and the SMP bit of the SSPSTAT register is set, then the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

5. Module: MSSP SPI

In SPI Master mode, if the SSPBUF register is written while a byte is actively being transmitted, an extra clock pulse will be improperly generated at the end of the transmission. Further writes to the SSPBUF register will be inhibited although 8 or 9 clock pulses will be generated for each attempted write. The WCON bit of the SSPCON register is properly set indicating that a write collision occurred. However, the write collision condition can only be cleared by resetting the MSSP module. Clear the MSSP by clearing the SSPEN bit of the SSPCON1 register.

Work around

Use the SSPIF bit of the PIR1 register or the BF bit of the SSPSTAT register to determine that the transmission is complete before writing the SSPBUF register. In the event that a write collision does occur, use the slave select feature to resynchronize the slave clock.

6. Module: MSSP I²C™

In Master I²C Receive mode if a Stop condition occurs in the middle of an address or data reception, then the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. If a Start condition occurs after the improper Stop condition then 9 additional clocks will be generated followed by the RCEN bit going low.

Work around

Use low impedance pull-ups on the SDA line to reduce the possibility of noise glitches which may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and resulting stuck RCEN bit. Clear the stuck RCEN bit by clearing the SSPEN bit of SSPCON1.

7. Module: EUSART

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

8. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/16th of a bit time is received. The RCIDL bit will then properly go high 1/8th of a bit time later. However, if another invalid Start bit occurs less than 1 bit time after the leading edge of the first invalid Start bit, then the RCIDL bit will improperly stay high then improperly go low one bit time later. The RCIDL bit will then stay low improperly until a valid Start bit is received.

Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

9. Module: Data EEPROM Memory

The write/erase endurance of Data EE Memory is limited to 10K cycles.

Work around

Use error correction method that stores data in multiple locations.

10. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when V_{DD} is above 3V. Endurance degrades when V_{DD} is below 3V.

Work around

For data tables in program Flash memory use error correction method that stores data in multiple locations.

Clarifications/Corrections to the Data Sheet:

1. Module: MSSP I^2C™

All entries in Table 17-3 with BRG values less than 0x03 are deleted. Add the following sentence to the end of Section 17.4.7:

The minimum SSPADD value for baud rate generation is 0x03.

2. Module: ADC

Equation 19-1: Change all occurrences of “MS” in the last two lines to “μs”.

3. Module: Interrupts

In Figure 9-1 remove the two-input OR gate in the middle of the diagram which has IPEN and GIEL/PEIE as the two inputs. Set the resulting floating output to ‘1’. This removes the requirement that PEIE be set for a peripheral to wake the device from Sleep when IPEN is low.

APPENDIX A: REVISION HISTORY

Rev. A Document (12/2008)

Initial release of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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