2M x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— 180 mW (max.)**
- **Operating voltages of 3.3 ± 0.3V**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$ and CE_2 features**

Functional Description

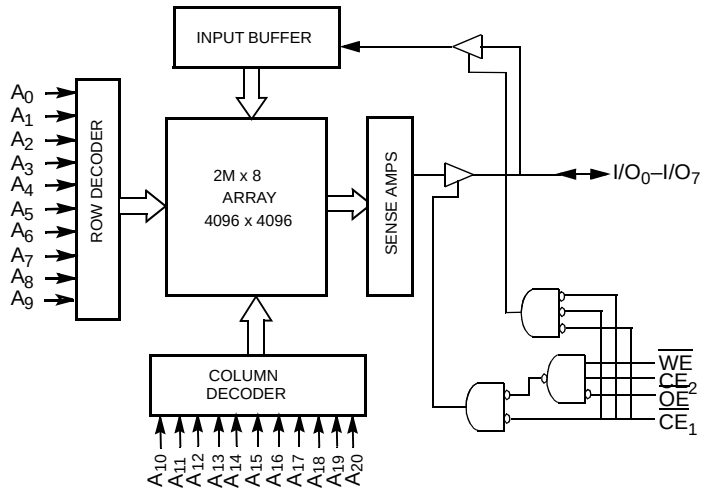
The CY7C1069AV33 is a high-performance CMOS Static RAM organized as 2,097,152 words by 8 bits. Writing to the device is accomplished by enabling the chip (by taking $\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW.

Reading from the device is accomplished by enabling the chip ($\overline{CE}_1$ LOW and CE_2 HIGH) as well as forcing the Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

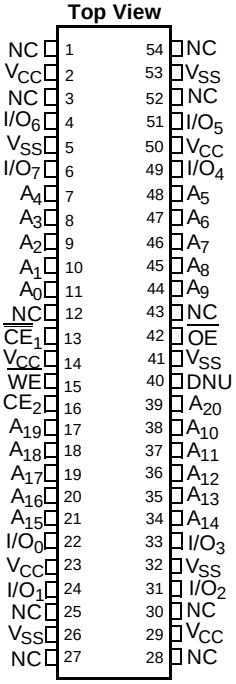
The CY7C1069AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 48-ball fine-pitch ball grid array (FBGA) package.

Logic Block Diagram



Pin Configuration

TSOP II
Top View



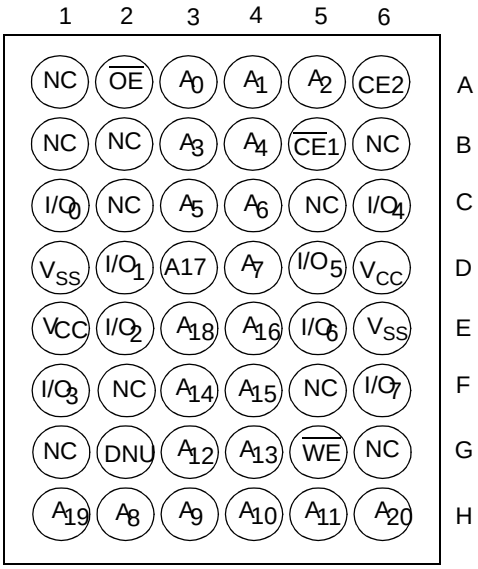
Selection Guide

		-10	-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Commercial	250	225	mA
	Industrial	250	225	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	mA

Pin Configurations

48-ball FBGA

(Top View)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[1] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1] .....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Commercial		250		225	mA
			Industrial		250		225	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	CE_2 ≤ V_{IL}, Max. V_{CC}, $\overline{SCE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			100		100	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	CE_2 ≤ 0.3V Max. V_{CC}, CE ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Commercial/ Industrial		50		50	mA

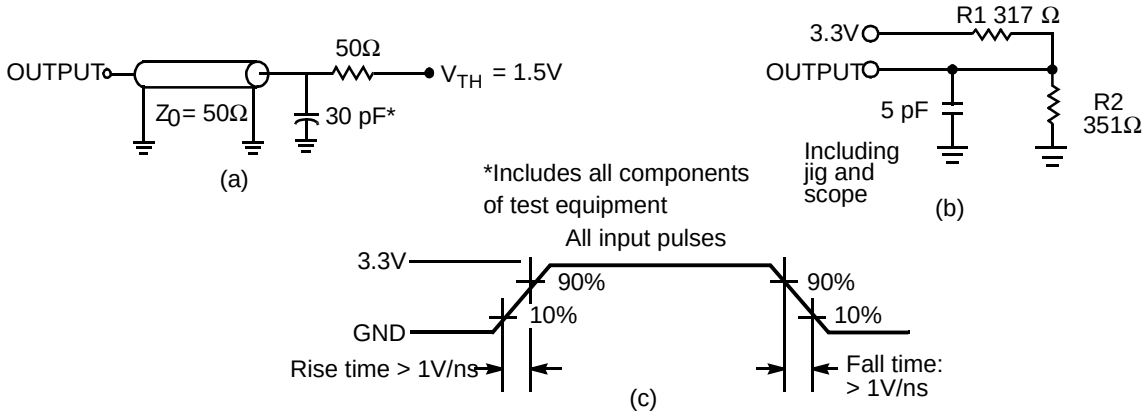
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	pF
C_{OUT}	I/O Capacitance		8	pF

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



AC Switching Characteristics Over the Operating Range [3]

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{power}	V_{CC}(typical) to the first access[4]	1		1		µs
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW / CE_2 HIGH to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[5, 6]	1		1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[5, 6]		5		6	ns
t_{LZCE}	$\overline{CE}_1$ LOW / CE_2 HIGH to Low-Z[5, 6]	3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH / CE_2 LOW to High-Z[5, 6]		5		6	ns
t_{PU}	$\overline{CE}_1$ LOW / CE_2 HIGH to Power-up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH / CE_2 LOW to Power-down		10		12	ns
Write Cycle[7, 8]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}_1$ LOW / CE_2 HIGH to Write End	7		8		ns
t_{AW}	Address Set-up to Write End	7		8		ns

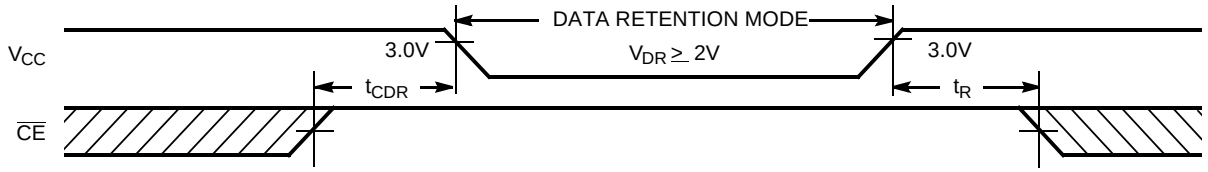
Notes:

3. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
4. This part has a voltage regulator which steps down the voltage from 3V to 2V internally. t_{power} time has to be provided initially before a Read/Write operation is started.
5. t_{HZOE}, t_{HZSCE}, t_{HZWE} and t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZSCE} is less than t_{LZSCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal Write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW / CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW along with CE_2 HIGH to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
8. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

AC Switching Characteristics Over the Operating Range (continued)[3]

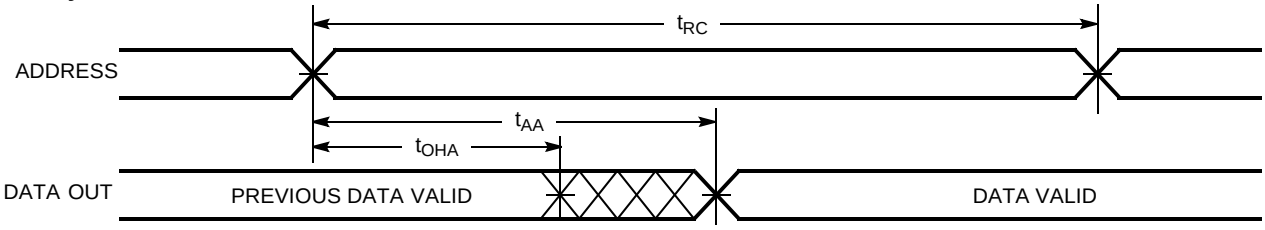
Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Set-up to Write End	5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[5, 6]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[5, 6]		5		6	ns

Data Retention Waveform



Switching Waveforms

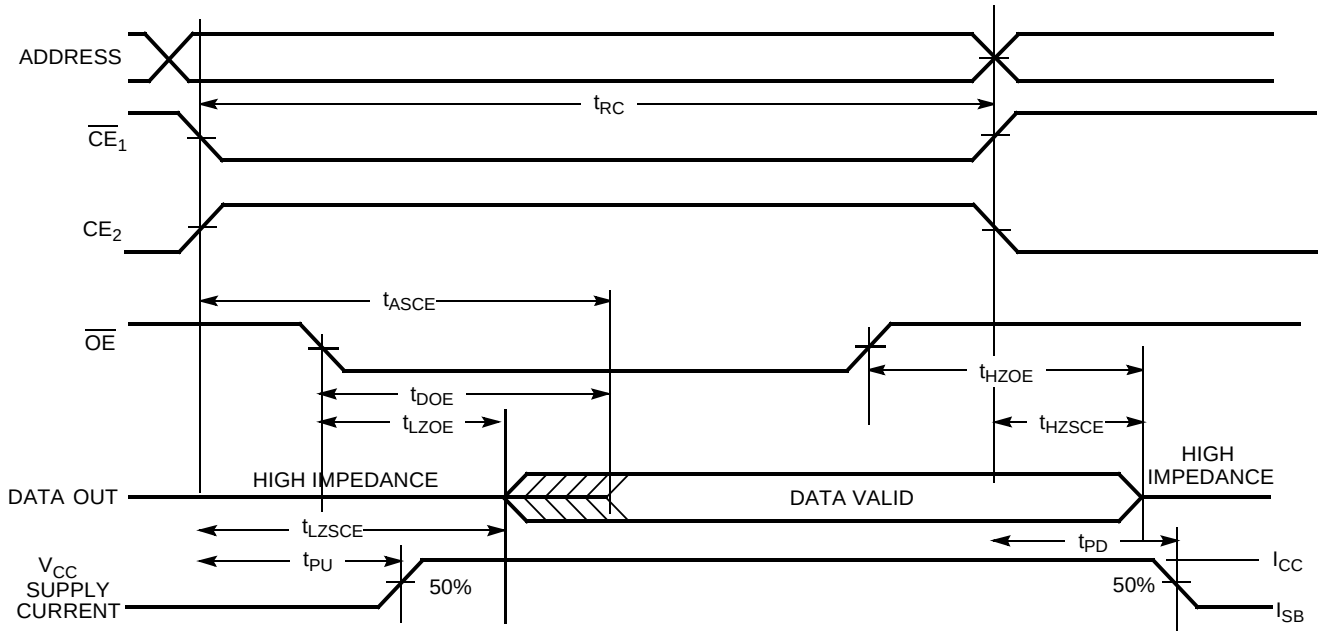
Read Cycle No. 1[9, 10]



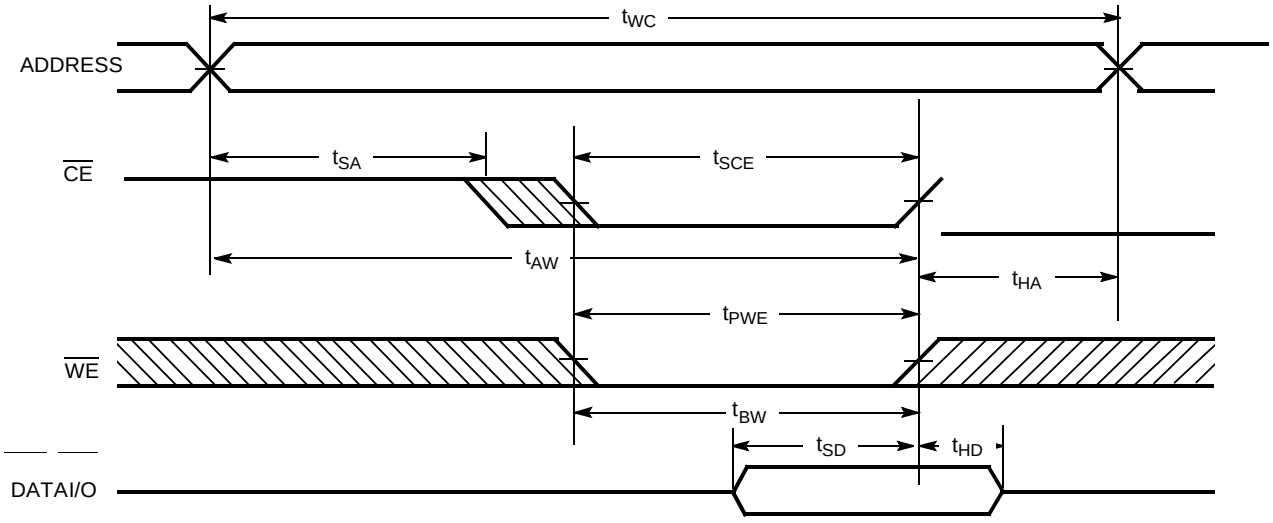
Notes:
9. Device is continuously selected. $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
10. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled) [10, 11]



Write Cycle No. 1 ($\overline{CE_1}$ Controlled) [12, 13, 14]

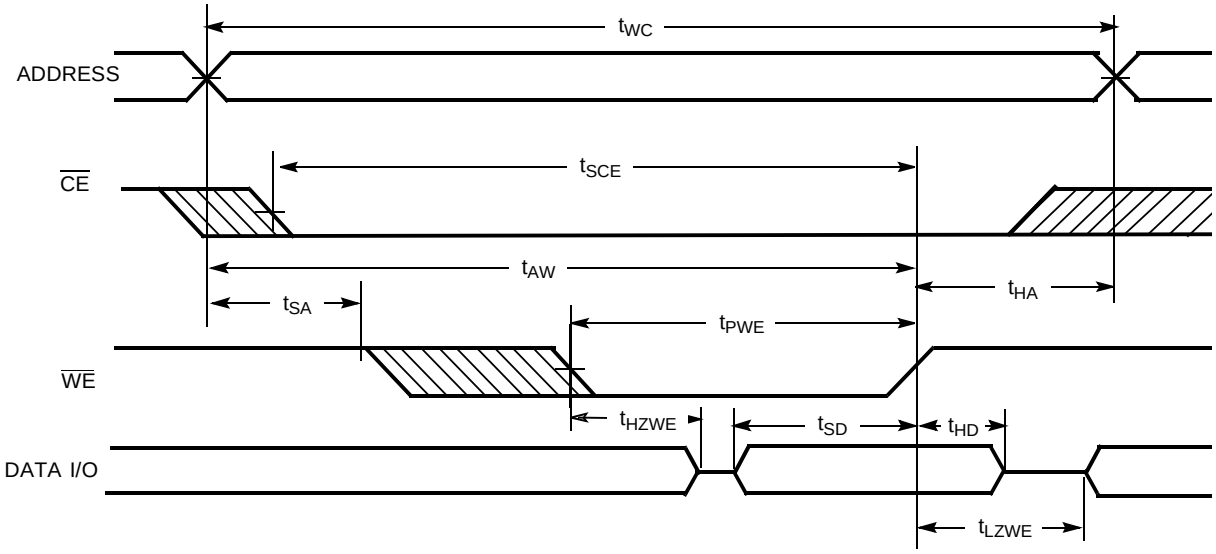


Notes:

11. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
12. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
13. If $\overline{CE_1}$ goes HIGH / CE_2 LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high–impedance state.
14. $\overline{CE}$ above is defined as a combination of $\overline{CE_1}$ and CE_2. It is active low.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, [12, 13, 14]



Truth Table

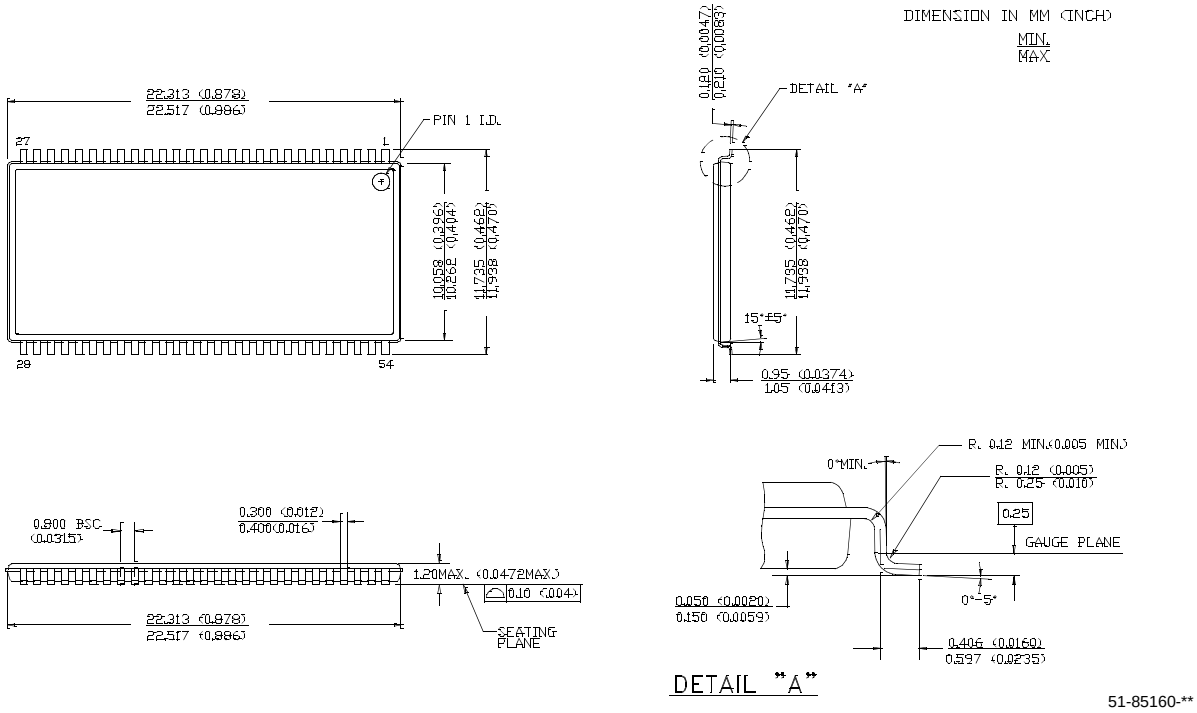
$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High-Z	Power-down	Standby (I_{SB})
X	L	X	X	High-Z	Power-down	Standby (I_{SB})
L	H	L	H	Data Out	Read All Bits	Active (I_{CC})
L	H	L	H	Data Out	Read Lower Bits Only	Active (I_{CC})
L	H	L	H	High-Z	Read Upper Bits Only	Active (I_{CC})
L	H	X	L	Data In	Write All Bits	Active (I_{CC})
L	H	X	L	Data In	Write Lower Bits Only	Active (I_{CC})
L	H	X	L	High-Z	Write Upper Bits Only	Active (I_{CC})
L	H	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1069AV33-10ZC	Z54	54-pin TSOP II	Commercial
	CY7C1069AV33-10ZI			Industrial
	CY7C1069AV33-10BAC	BA48	48-ball Mini BGA	Commercial
	CY7C1069AV33-10BAI			Industrial
12	CY7C1069AV33-12ZC	Z54	54-pin TSOP II	Commercial
	CY7C1069AV33-12ZI			Industrial
	CY7C1069AV33-12BAC	BA48	48-ball Mini BGA	Commercial
	CY7C1069AV33-12BAI			Industrial

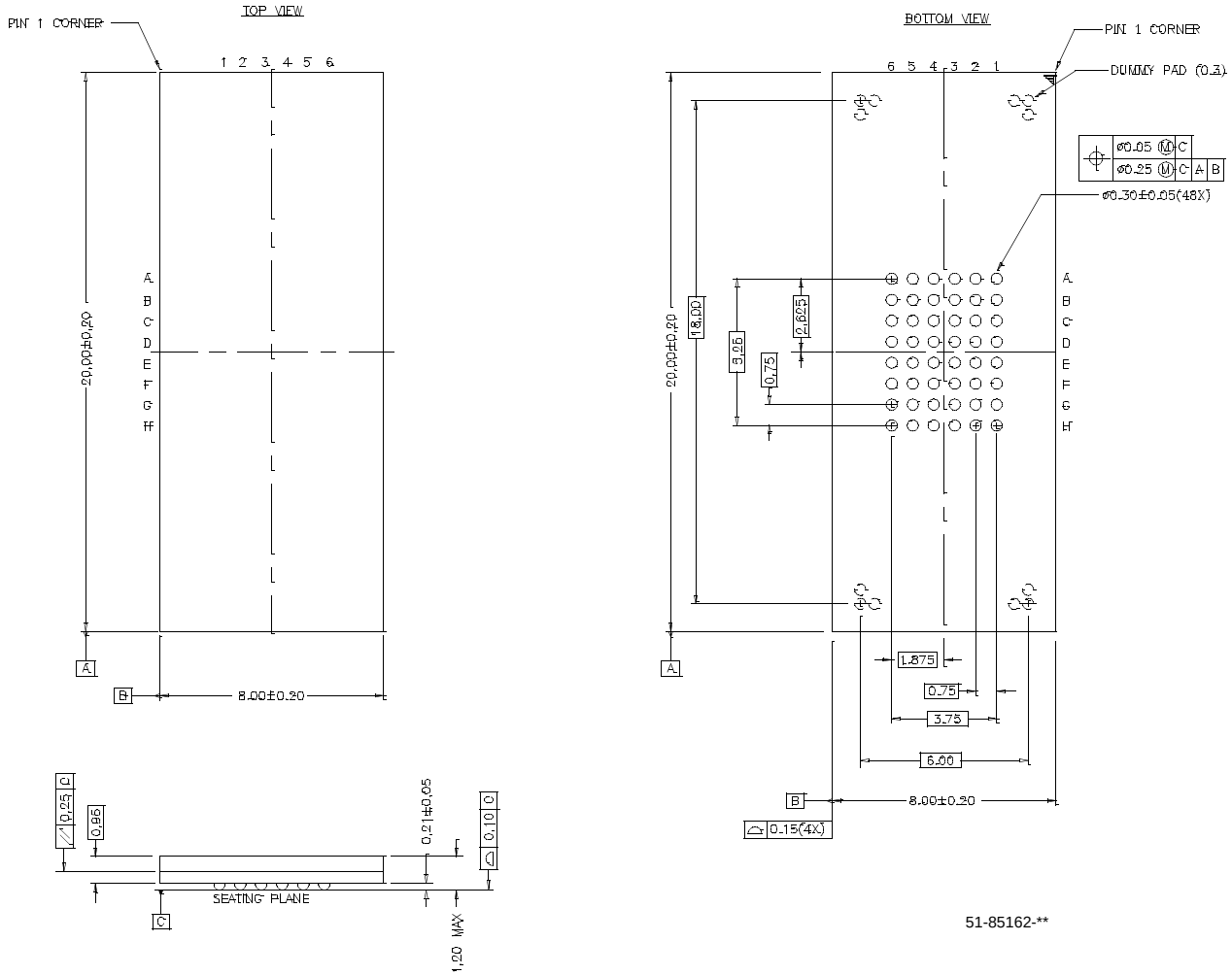
Package Diagrams

54-lead Thin Small Outline Package, Type II Z54-II



Package Diagrams (continued)

48-ball (8 mm x 20 mm x 1.2 mm) FBGA BA48G



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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113724	03/27/02	NSL	New Data Sheet
*A	117060	07/31/02	DFP	Removed 15 ns bin.