

PIC16F785 Rev. A Silicon/Data Sheet Errata

The PIC16F785 parts you have received conform functionally to the Device Data Sheet (DS41249B), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the PIC16F785 silicon.

1. Module: Two-Phase PWM (Complementary Mode)

The Complementary mode is not supported due to the nature and extent of the Complementary mode anomalies. Complementary mode in the A1 silicon should be used for evaluation purposes only.

1. Duty cycle by comparator feedback (COMOD = X1) is not supported.
2. When the duty cycle is determined by the difference between the PH1 and PH2 phase delays (CMOD = 10), both outputs can sometimes hang low if the duty cycle is less than 20 ns or greater than the phase switching dead time. The hang condition can only be cleared by setting the dead time to zero.
3. Maximum phase switching dead time is limited by the PWM clock frequency (`pwm_clock`). At a `pwm_clock` frequency of 20 MHz, the maximum dead time is about 35 ns. At a `pwm_clock` frequency of 10 MHz, the maximum dead time is about 80 ns. The relationship between maximum dead time and `pwm_clock` frequency is approximately linear.
4. The shutdown condition will correctly force PH1 false (low output at PH1 flop before the inverting XOR gate). PH2 will be incorrectly forced true (high output at PH2 flop before inverting XOR gate).
5. If the dead time is not zero and `PWMPH1<4:0> = PWMPH2<4:0>` then both phase outputs will be driven false (PH1 and PH2 low before inverting XOR gate). If the dead time is zero and `PWMPH1<4:0> = PWMPH2<4:0>`, then phase 1 will be driven true (PH2 high) for all but one `pwm_clock` cycles every PWM period.

Work around

None.

2. Module: Two-Phase PWM (Two-Phase Mode)

1. If the PWMASE bit is set when the PASEN bit is cleared, then the PWMASE bit will be stuck high and the PWM will be frozen in shutdown. Shutdown can only be cleared by first setting the PASEN bit high then clearing the shutdown condition (RA2/INT input must be high) so the PWMASE bit can be cleared.
2. In normal two-phase operation when the output is inverted, the leading edge is delayed by about 10 ns and the trailing edge occurs about 7 ns early. When the phase delay is set to maximum, the leading edge is delayed about 8 ns. The net result of these two phenomena is that at 20 MHz `Fosc`, a blanked inverted output at maximum phase delay will not be generated.

Work around

None.

3. Module: Capture/Compare/PWM (CCP)

The first capture will occur one edge too early if the RC5/CCP1 input is high when selecting the CCP mode to capture either every 4th edge (`CCP1CON<3:0> = 0110`) or every 16th edge (`CCP1CON<3:0> = 0111`). Subsequent captures will occur properly.

Work around

None.

4. Module: Capture/Compare/PWM (CCP)

Reading bit 5 of PORTC (RC5/CCP1) always returns a '0' when the CCP module is configured for any of the four capture modes (`CCP1CON<3:0> = 01xx`). This condition is true when the RC5/CCP1 pin is configured as either an input (`TRISC<5> = 1`) or output (`TRISC<5> = 0`). When configured as an output, the ability to set the RC5/CCP1 pin high or low works normally although reading the pin status always returns '0'.

Work around

None.

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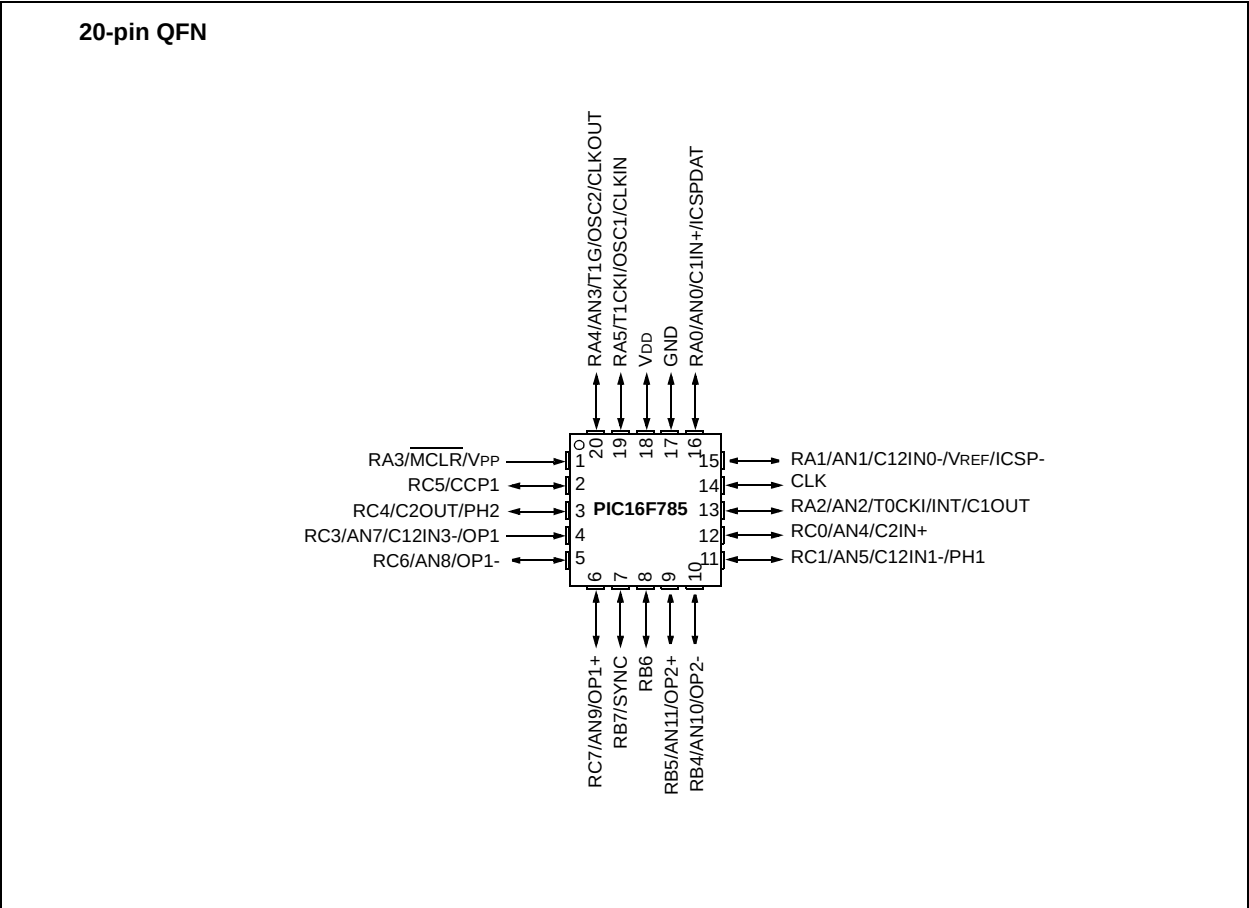
Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (41249B), the following clarifications and corrections should be noted.

1. Module: New 4x4 QFN Package Added

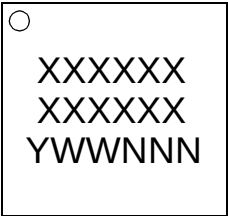
The new 20-pin 4x4 QFN pinout diagram will be added to the Pin Diagrams figure on page 2 and the Packaging Information chapter as shown below:

Pin Diagram

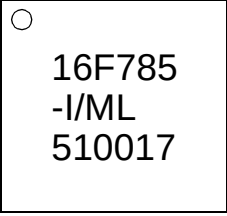


14.1 Package Marking Information

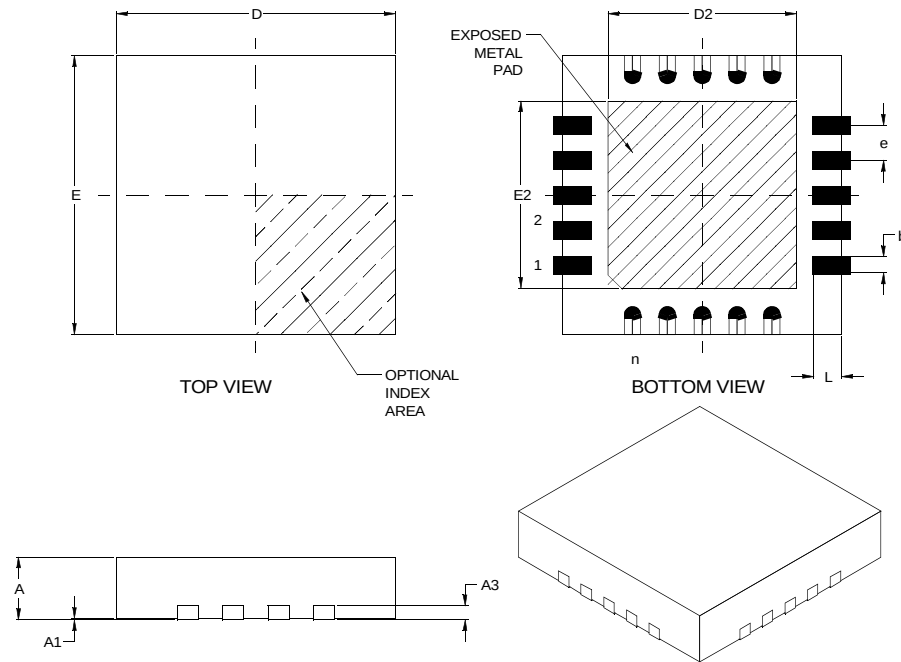
20-Lead QFN



Example



20-Lead Plastic Quad Flat No Lead Package (ML) 4x4x0.9 mm Body (QFN) – Saw Singulated



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	20			20		
Pitch	e	.020 BSC			0.50 BSC		
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3	.008 REF			0.20 REF		
Overall Width	E	.152	.157	.163	3.85	4.00	4.15
Exposed Pad Width	E2	.090	.104	.106	2.29	2.64	2.69
Overall Length	D	.152	.157	.163	3.85	4.00	4.15
Exposed Pad Length	D2	.090	.104	.106	2.29	2.64	2.69
Contact Width	b	.007	.010	.012	0.18	0.25	0.30
Contact Length	L	.012	.016	.020	0.30	0.40	0.50

*Controlling Parameter

Notes:

1. BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M
2. REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

Exposed pad varies according to die attach paddle size.

JEDEC equivalent: Not Registered

Drawing No. C04-126, Revised 05-05-05

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REVISION HISTORY

Rev A Document (4/2005)

First release of document. Added Module 1, "Two-Phase PWM" and Module 2, "Two-Phase Mode".

Rev B Document (5/2005)

Added item #5 and #6 to Module 1, "Two-Phase PWM (Complementary mode)".

Rev C Document (7/2005)

Clarifications/Corrections to the Data Sheet:

Added Module 1, New 4x4 QFN Package added.

Rev D Document (12/2005)

Added Modules 3 and 4, "Capture/Compare/PWM (CCP)".

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