PIC16F631/677/685/687/689/690 Rev. A Silicon/Data Sheet Errata

The PIC16F631/677/685/687/689/690 parts you have received conform functionally to the Device Data Sheet (DS41262**E**), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC16F631/677/685/687/689/690 silicon.

1. Module: EUSART (PIC16F687/689/690 only)

1.1 WUE Bit is not clearing.

After a wake-up due to a Break character, the WUE bit is not automatically cleared.

Work around

Clear the WUE bit after waking up.

Fix

Rev. A5 Silicon and later revisions.

1.2 Auto-baud captures the incorrect baud rate after a break.

The SPBRGH:SPBRG registers are not being initialized correctly. If WUE and ABDEN are set at the same time and a Break character followed by a Sync character are received, then the calculated baud rate will be random.

Work around

Set WUE and wait for the wake-up to occur.

Clear SPBRGH:SPBRG after waking up with the break.

Set ABDEN to begin the auto-baud process.

Fix

Rev. A5 Silicon and later revisions.

1.3 Auto-baud calculates a baud rate value that is +2.

The SPBRGH:SPBRG are not initialized correctly when ABDEN is set. This causes the measured baud rate to be high by two counts.

Work around

Clearing the SPBRGH:SPBRG registers will correctly initialize the baud rate counter. After the auto-baud has been completed, the baud rate will now be +1. The firmware should now subtract 1 from the Baud Rate Generator to produce the correct baud rate.

Fix

Rev. A5 Silicon and later revisions.

1.4 Delay after auto-baud before transmit is allowed.

After the auto-baud Sync character has been received and the RCIF flag is set, there is approximately 17 ms of delay before the transmitter is enabled.

Work around

After the RCIF flag is set indicating the baud rate has been measured, read the SPBRG register and write the value back to SPBRG. This will terminate the delay, and enable the transmitter module.

Fix

Rev. A5 Silicon and later revisions.

1.5 Auto-baud sequence cannot be aborted in some cases.

If an auto-baud is started but no edges are received, there is no way to leave Auto-Baud mode.

Work around

Use the Watchdog Timer to reset the entire device.

Fix

Rev. A5 Silicon and later revisions.

1.6 Clearing SPEN does not reset EUSART state machine correctly.

When SPEN is cleared, the entire EUSART is frozen. When SPEN is set, the EUSART resumes where it left off. This can cause some unexpected behavior.

Work around

To reset the EUSART, toggle TXEN and CREN after clearing SPEN. This will reset the transmit and receive state machines.

Fix

Rev. A5 Silicon and later revisions.

1.7 Extra character transmitted after auto-baud.

If TXEN is high when ABDEN is set, it will be cleared as soon as the auto-baud process begins, and reset as soon as the auto-baud process completes. When TXEN is reset, the character in the transmit queue will be transmitted.

Work around

Before starting auto-baud, clear TXEN. This will reset the transmit state machine correctly. After the auto-baud is complete and the firmware has brought TXEN high, no character will be transmitted.

Fix

Rev. A5 Silicon and later revisions.

2. Module: SSP (PIC16F687/689/690 only)

2.1 SSP module does not recognize first Start bit received.

In any of the I^2C™ modes, the SSP module will fail to recognize the first Start bit received after a transition from module disable to module enable. Subsequent Stop bits and Start bits are detected properly.

Work around

Enable the SSP module in SSPMSK Access mode before changing the mode to the desired I^2C operation.

EXAMPLE 1: CODE EXAMPLE

```
MOVLW  B'00111001'  ;Module enable, clock
MOVWF  SSPCON       ;enable, SSPMSK access.
                    ;Optionally load
                    ;address mask value
                    ;into SSPMSK register.
MOVLW  B'00110110'  ;Module enable, clock
MOVWF  SSPCON       ;enable, 7-bit address
                    ;I2C slave.
```

Fix

Rev. A6 Silicon and later revisions.

2.2 Under certain conditions, the SSPIF flag sets on reception of the first byte.

When all of the following conditions are met:

- The module is configured as a SPI slave
- CKP = 1
- CKE = 1
- Multiple bytes are sent with the $\overline{SS}$ line remaining low between bytes

The SSPIF flag will only be set on reception of the first byte and the following bytes will not be correctly received.

Work around

- Toggle the $\overline{SS}$ line between bytes

or

- On reception of the first byte modify the SSPM bits in the SSPCON register to configure the module as a SPI slave with $\overline{SS}$ pin disabled. Then restore the SSPM bits to the configuration for SPI slave with $\overline{SS}$ pin enabled. The module is then ready for reception of the following byte.

Fix

None.

3. Module: ECCP with Auto-Shutdown (Silicon Rev. A4 and previous revisions) (PIC16F685 and PIC16F690 only)

The PIC16F631/677/685/687/689/690 Rev. A4 silicon for the ECCP auto-shutdown is connected to the C1IF and C2IF flags. See Figures 8-2 and 8-3 on the following page.

The auto-shutdown connection (Rev. A4 and previous) to C1IF and C2IF causes the auto-shutdown to incorrectly operate synchronously. Additionally, reads of CMxCON0 will incorrectly clear an auto-shutdown event.

Work around

Rev. A4 Silicon and previous revisions.

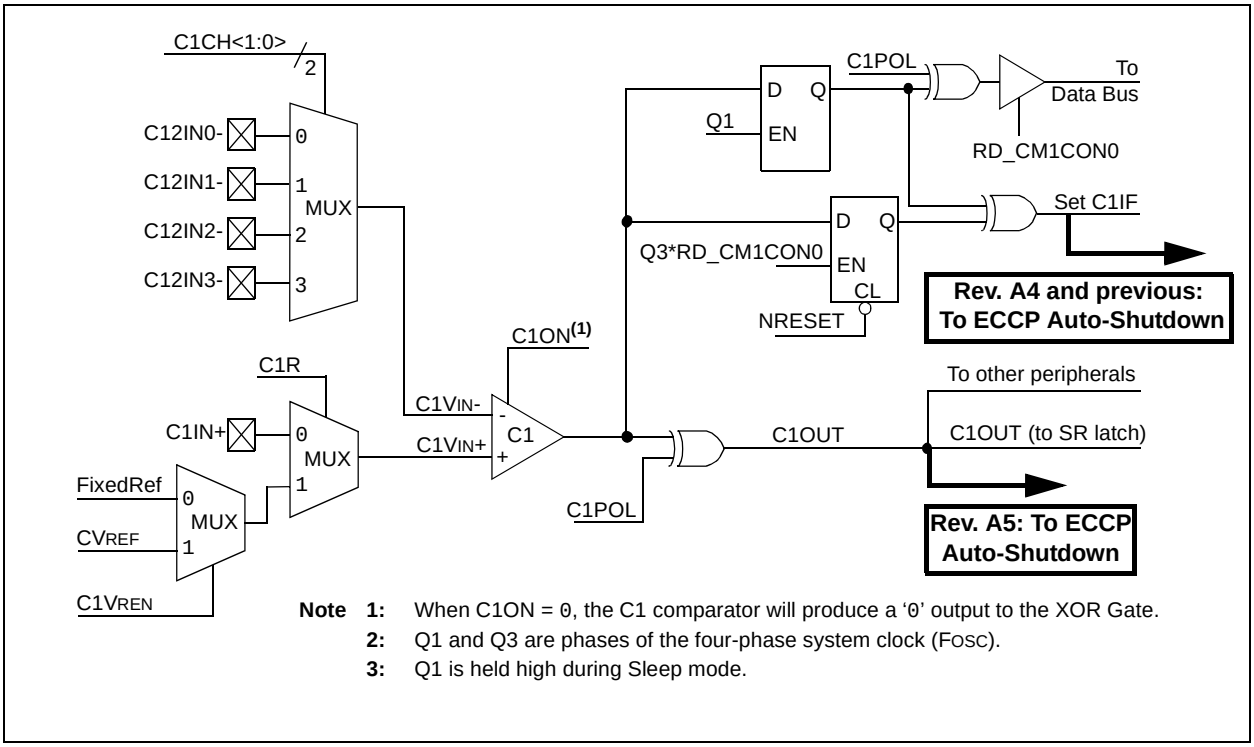
1) Poll the CxOUT bit until it is low.
2) Read CMxCON0 to precondition CxIF.
3) If CMxCON0 is read while CxOUT is changing, repeat steps 1 and 2.

Fix

Rev. A5 Silicon and later revisions.

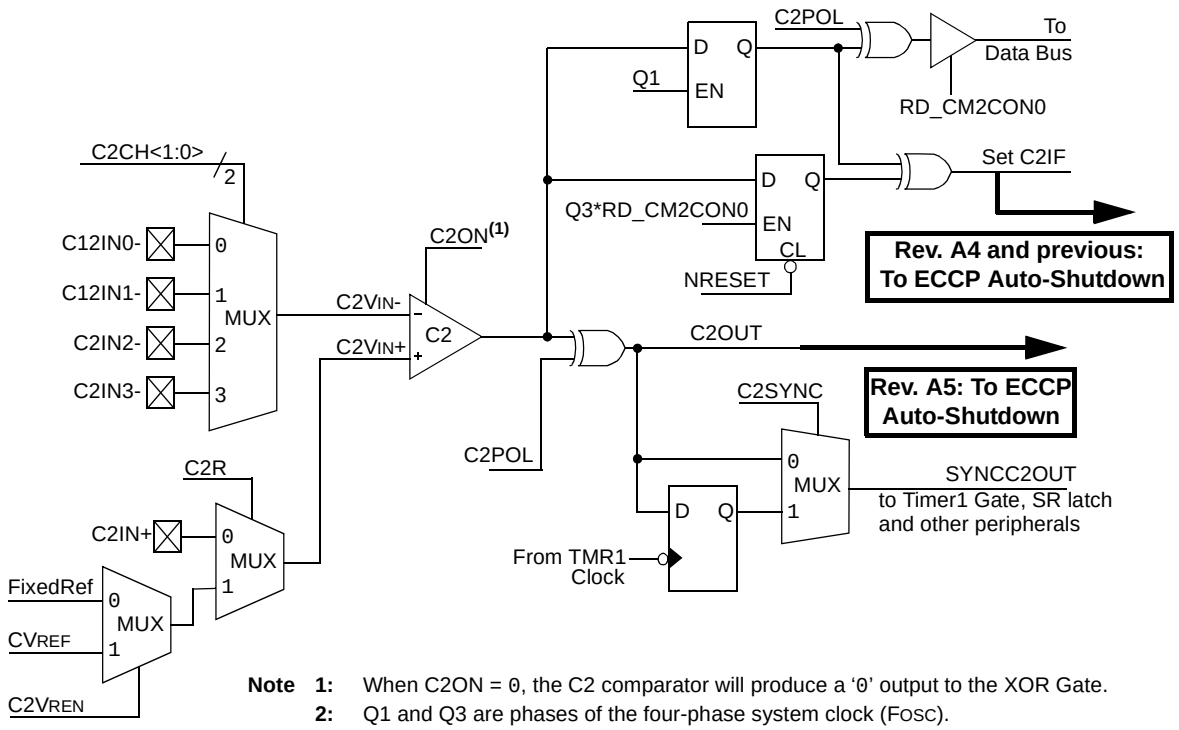
The Silicon Rev. A5 (now shipping) and later revision devices have moved the auto-shutdown connection from CxIF to CxOUT. This will eliminate the synchronous shutdown and simplify the use of the comparator for a shutdown event. Figure 1 shows the function of auto-shutdown before and after the device revision.

FIGURE 8-2: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM



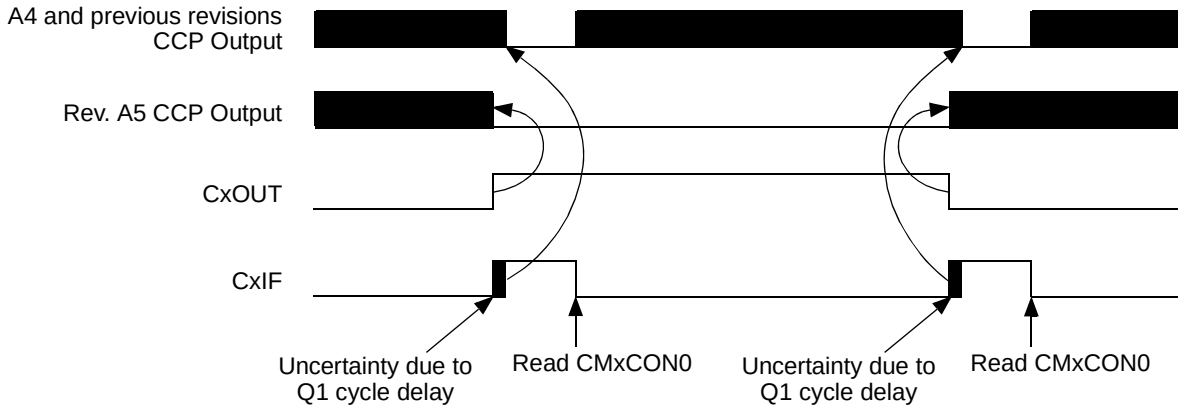
Note 1: When C1ON = 0, the C1 comparator will produce a '0' output to the XOR Gate.
2: Q1 and Q3 are phases of the four-phase system clock (FOSC).
3: Q1 is held high during Sleep mode.

FIGURE 8-3: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C2ON = 0, the C2 comparator will produce a '0' output to the XOR Gate.
2: Q1 and Q3 are phases of the four-phase system clock (FOSC).
3: Q1 is held high during Sleep mode.

FIGURE 1: SILICON REVISION A4 AND PREVIOUS VS. REVISION A5



4. Module: Analog-To-Digital Converter (ADC) Module (PIC16F685/687/689/690 Only)

Selecting the VP6 reference as the analog input source (CHS<3:0> = 1101) for the ADC conversion after sampling another analog channel with input voltages approximately greater than 1.2V can temporarily disturb the HFINTOSC oscillator.

Note:	This only occurs when selecting the VP6 reference ADC channel using the CHS<3:0> bits in the ADCON0 register and NOT during the start of an actual ADC conversion using the GO/DONE bit in the ADCON0 register.

Work around

Select an ADC channel with input voltages lower than 1.2V prior to selecting the VP6 reference voltage input. Any analog channel can be used, even if that channel is configured as a digital I/O (configured as an output) that is driving the output pin low. An alternative is to configure the CV_{REF} module to output a voltage less than 1.2V and then selecting that analog channel CHS<3:0> = 1100 as the analog input source.

EXAMPLE 2: AVOID DISTURBING THE HFINTOSC OSCILLATOR

```
BANKSEL    ADCON0        ;
MOVLW      B'XX110001'   ;Select ADC
MOVWF      ADCON0        ;Channel CVREF
MOVLW      B'XX110101'   ;Select ADC
MOVWF      ADCON0        ;Channel VP6
```

Silicon Fix

None.

5. Module: LP/Timer1 Oscillator Operation Below 25°C

At temperatures below 25°C, the shared LP and Timer1 external 32 kHz Oscillator module may have reduced oscillator peak-to-peak voltage with decreasing temperature.

This can cause irregular Timer1 overflow or instruction execution and in extreme cases, oscillations may stop.

The same issue may also prevent the external 32 kHz oscillator from starting up at low temperatures.

Work around

Adding an external 1 MOhm pull-up resistor on OSC2 allows the oscillator to start and run successfully over its operating temperature range.

Silicon Fix

None.

6. Module: SSP (PIC16F687/689/690)

When all of the following conditions are met:

1. The module is configured as a SPI slave
2. CKP = 1
3. CKE = 1
4. Multiple bytes are sent with the SS line remaining low between bytes

The SSPIF flag will only be set on reception of the first byte and the following bytes will not be correctly received.

Work around

- Toggle the SS line between bytes

or

- On reception of the first byte modify the SSPM0 bit in the SSPCON register to configure the module as a SPI slave with SS pin disabled. Then restore the SSPM0 bit to the configuration for SPI slave with SS pin enabled. The module is then ready for reception of the following byte.

```
bsf SSPCON, SSPM0
bcf SSPCON, SSPM0
```

Silicon Fix

None.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41262**E**), the following clarifications and corrections should be noted.

None.

REVISION HISTORY

Rev A Document (7/2005)
Original release of this document.
Clarifications/Corrections to the Data Sheet:
Added Modules 1 through 7:
Module 1: Device V_{DD} Range
Module 2: 4x4 QFN Package Marking
Module 3: Table 1-1: Pinout Description – PIC16F685
Module 4: Register 10-5: EECON1
Module 5: Table11-2: Registers Associated with Capture, Compare and Timer1
Module 6: Section 12.0 EUSART
Module 7: Section 14.2.2 $\overline{MCLR}$

Rev B Document (8/2005)
Silicon Section:
Added Module 1: EUSART (PIC16F687/689/690 only).

Clarifications/Corrections to the Data Sheet:
Added Modules 8 and 9:
Module 8: SSP Module Overview
Module 9: Electrical Specifications.

Rev C Document (11/2005)
Silicon Section:
Added Module 2: SSP (PIC16F687/689/690 only)

Rev D Document (01/2006)

Clarifications/Corrections to the Data Sheet:

Replaced the 20-Lead QFN package diagram in Module 2: 4x4 QFN Package Marking.

Rev E Document (7/2006)
Data Sheet Clarifications/Corrections Section: Removed Items 1 through 9, which have been incorporated into the data sheet. Added Item 1, 20-pin QFN Pin Diagram Title change.

Rev F Document (11/2006)
Data Sheet Clarifications/Corrections Section: Added Item 2, Product Identification System, Examples change.

Added Module 3: ECCP with Auto-Shutdown (Silicon Rev. B2). Updated Module1: EUSART (PIC16F687/689/690 only) and Module2: SSP (PIC16F687/689/690 only) with Fix information.

Rev G Document (01/2007)
Removed Rev. A6 reference from Module 2 (SSP).

Data Sheet Clarifications/Corrections Section: Added Module 3, Comparator and Voltage Reference Modules Associated Registers, removed REFCON register reference. Added Module 4: DC Characteristics, Table 17.3, revised Max values.

Rev H Document (07/2007)
Added Module 4: Analog-to-Digital Converter (ADC) Module. Module 2: Added Fix.

Rev J Document (09/2008)
Added Module 2.2: Under certain conditions, the SSPIF flag sets on reception of the first byte (under new 2. SSP (PIC16F687/689/690 only)), while changing Module 2. to 2.1. Revised Module 5: LP/Timer1 Oscillator Operations Below 25°C. Added Module 6: SSP.

Clarifications/Corrections to the Data Sheet:
Removed Modules 1 through 4, which have been included in the latest data sheet revision.

NOTES:

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