

PIC16F636/639 Rev. A Silicon/Data Sheet Errata

The PIC16F636/639 parts you have received conform functionally to the Device Data Sheet (DS41232C), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the **PIC16F636/639** devices.

1. Module: Resets (when WDT times out)

If the OPTION_REG bits: PS<2:0> are changed from any other value to '000', multiple spurious Resets can occur when the WDT times out. These Resets can occur even when the PSA bit is clear, assigning the prescaler to the Timer0.

Work around

If a CLRWDI instruction is issued before the WDT times out and before the OPTION register PS<2:0> bits are modified, this problem is eliminated.

This issue was corrected in revision B silicon.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Wake-up Reset (WUR)

If a Wake-up Reset occurs when the Wake-up Reset (WURE) and Power-up Timer (PWTRE) Configuration bits are enabled in revision A silicon, there will not be a 72 ms time delay as expected.

Work around

There is no work around in revision A silicon for this errata. However, this issue was corrected for revision B silicon. If a Wake-up Reset occurs when the Wake-up Reset and Power-up Timer Configuration bits are enabled in revision B silicon, there will be a nominal 72 ms time delay following the Wake-up Reset.

3. Module: Internal/External Clock Switch Over (IESO)

If a Wake-up Reset occurs when the Wake-up Reset (WURE) and Internal/External Clock Switch Over (IESO) Configuration bits are enabled in revision A silicon and there is no external clock applied to the chip when in the XT/HS configurations, the processor will hang on a Wake-up Reset.

Work around

There is no work around in revision A silicon for this errata. However, this issue was corrected for revision B silicon. If a Wake-up Reset occurs when the Wake-up Reset and Internal/External Clock Switch Over Configuration bits are enabled in revision B silicon and a Wake-up Reset occurs, the chip will wake up and reset as expected.

4. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work around

1. Avoid operations on the PIR1 register when writing to the EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer Interrupt Service Routine to verify the EEPROM write success.
4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

Fix

Rev. B Silicon and later revisions.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41232C), the following clarifications and corrections should be noted.

None.

REVISION HISTORY

Rev A Document (8/2004)

Issue 1 – When OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out.

Added Clarifications/Corrections to the Data Sheet, Issues 1, 2 and 3 (changed to 8-pin MF **saw singulated** packaging).

Rev B Document (01/2005)

Added PIC16F639 device.

Revised Module 1: Resets.

Deleted Clarification/Corrections to the Data Sheet. Data Sheet has been updated.

Rev C Document (07/2005)

Data Sheet Clarifications/Corrections Section: Added Module 1: New 4x4 QFN Package added.

Rev D Document (02/2006)

Data Sheet Clarifications/Corrections Section: Added Module 2: I/O Pins.

Rev E Document (03/2006)

Data Sheet Clarifications/Corrections section: Added Module 3: Data EEPROM Memory; Added Module 4: Electrical Specifications. Replaced QFN Package Drawing.

Rev F Document (06/2006)

Added Module 2: "Wake-up Reset (WUR)", and Module 3: "Internal/External Clock Switch Over".

Rev G Document (11/2006)

Added Module 4: "Data EEPROM Memory".

Data Sheet Clarifications/Corrections section: removed all sections, data sheet updated (DS41232C).

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