

PIC16F506 Rev. B Silicon/Data Sheet Errata

The PIC16F506 parts you have received conform functionally to the Device Data Sheet (DS41268B), except for the anomalies described below.

All issues listed here will be addressed in future revisions of the silicon. Where noted, problems apply to listed revision only.

1. Module: Analog-to-Digital (A/D) Converter

The A/D Converter does not meet the design target. The specifications listed below in Table 1 supersedes Table 13-3 in DS41268B.

TABLE 1: A/D CONVERTER CHARACTERISTICS AT 8 BITS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A03	EIL	Integral Error	—	—	±2	LSb	V _{DD} = 5.0V 25°C
A04	EDL	Differential Error	—	—	-1 ≤ EDL ≤ 2	LSb	V _{DD} = 5.0V 25°C Supersedes conditions for Param. A04 (DS41268B)
A06	EOFF	Offset Error	—	—	±2	LSb	V _{DD} = 5.0V 25°C
A07	EGN	Gain Error	—	—	±2	LSb	V _{DD} = 5.0V 25°C
A25	VAIN	Analog Input Voltage	V _{SS} V _{SS}	— —	V _{DD} .9 V _{DD}	V V	T > 85°C and F _{osc} > 10 MHz only

* These parameters are characterized but not tested.

† Data in the “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only are not tested.

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FIGURE 1: TYPICAL DNL AT 2.0V (OPERATION AT 7-BIT LEVEL)

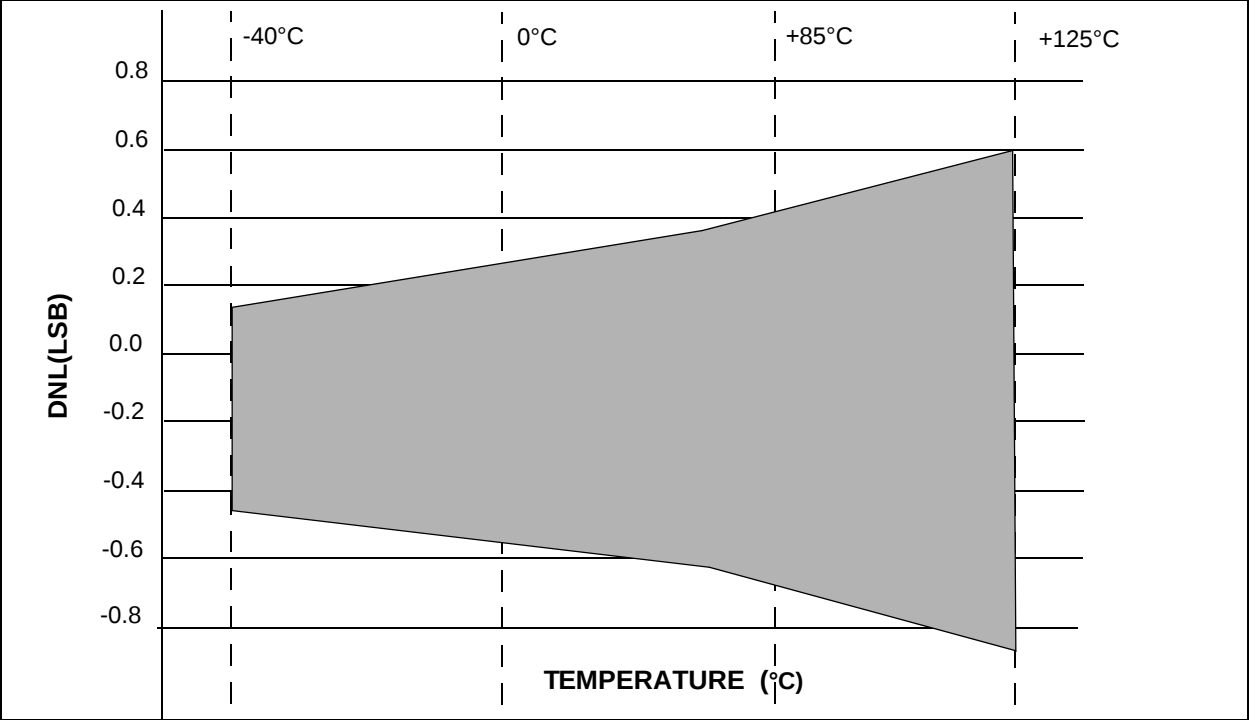


FIGURE 2: TYPICAL INL AT 2.0V (OPERATION AT 7-BIT LEVEL)

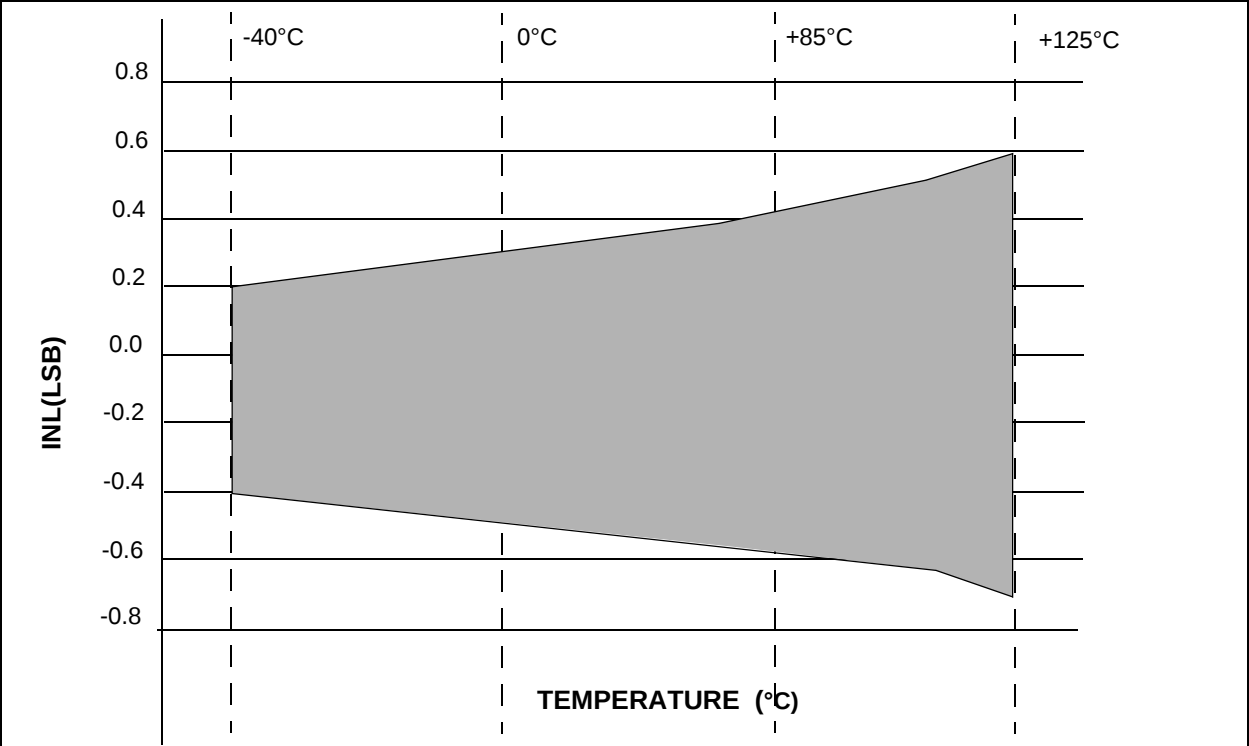


FIGURE 3: TYPICAL DNL AT 5.5V (OPERATION AT 7-BIT LEVEL)

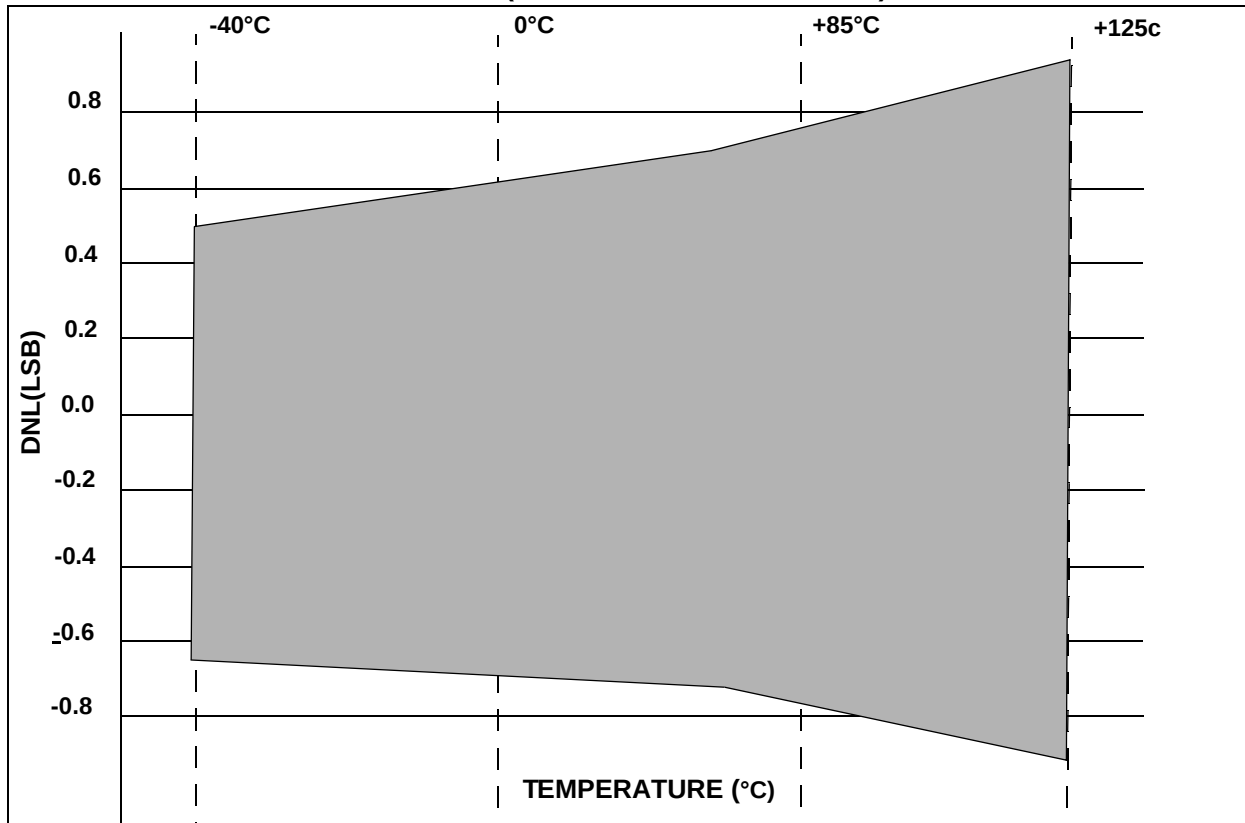
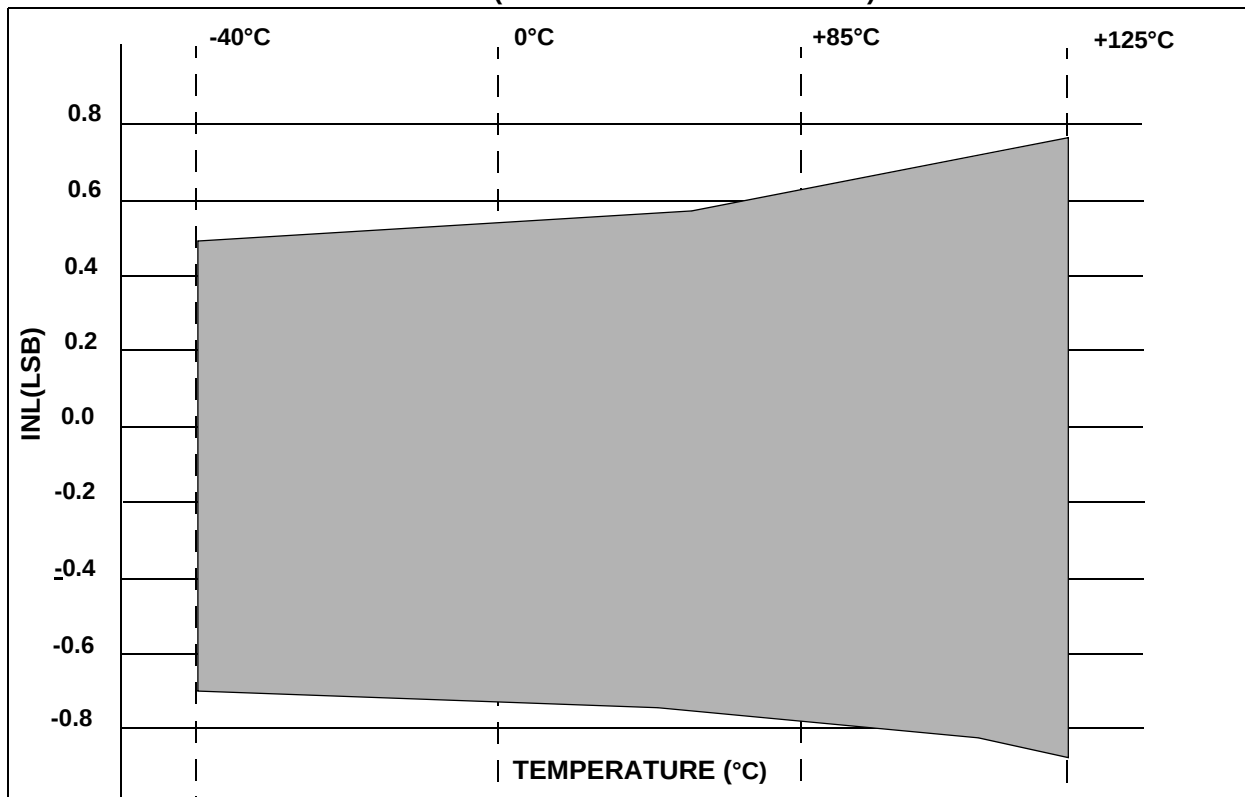


FIGURE 4: TYPICAL INL AT 5.5V (OPERATION AT 7-BIT LEVEL)



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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41268B), the following clarifications and corrections should be noted.

1. Module: Analog-to-Digital (A/D)

Table 9-2 TAD FOR ADCS SETTINGS WITH VARIOUS OSCILLATORS should read as follows:

TABLE 9-2: TAD FOR ADCS SETTINGS WITH VARIOUS OSCILLATORS

Source	ADCS <1:0>	Divisor	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz	500 kHz	350 kHz	200 kHz	100 kHz	32 kHz
INTOSC	11	4	—	—	.5 μ s	1 μ s	—	—	—	—	—	—
FOSC	10	4	.2 μ s	.25 μ s	.5 μ s	1 μ s	4 μ s	8 μ s	11 μ s	20 μ s	40 μ s	125 μ s
FOSC	01	8	.4 μ s	.5 μ s	1 μ s	2 μ s	8 μ s	16 μ s	23 μ s	40 μ s	80 μ s	250 μ s
FOSC	00	16	.8 μ s	1 μ s	2 μ s	4 μ s	16 μ s	32 μ s	46 μ s	80 μ s	160 μ s	500 μ s

TABLE 13-2: COMPARATOR VOLTAGE REFERENCE (VREF) SPECIFICATIONS

Sym	Characteristics	Min	Typ	Max	Units	Comments
CVRES	Resolution	—	VDD/24*	—	LSb	Low Range (VRR = 1)
		—	VDD/32	—	LSb	High Range (VRR = 0)
	Absolute Accuracy ⁽²⁾	—	—	$\pm 1/2^*$	LSb	Low Range (VRR = 1)
		—	—	$\pm 1/2^*$	LSb	High Range (VRR = 0)
	Unit Resistor Value (R)	—	2K*	—	Ω	
	Settling Time ⁽¹⁾	—	—	10*	μ s	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

2: Do not use reference externally when VDD < 2.7V. Under this condition, reference should only be used with comparator Voltage Common mode observed.

APPENDIX A: REVISION HISTORY

Rev A Document (01/2007)

First revision of this document.

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NOTES:

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