

PIC18F1220/1320 Rev. D0 Silicon/Data Sheet Errata

The PIC18F1220/1320 Rev. D0 parts you have received conform functionally to the Device Data Sheet (DS39605C), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC18F1220/1320 silicon.

The following silicon errata apply only to PIC18F1220/1320 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F1220	00 0111 111	00111
PIC18F1320	00 0111 110	00111

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Core (DAW Instruction)

The DAW instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as INCF SZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

MOVLW	0x80	; .80 (BCD)
ADDLW	0x80	; .80 (BCD)
BTFSC	STATUS, C	; test C
INCF SZ	byte2	; inc next higher LSB
DAW		
BTFSC	STATUS, C	; test C
INCF SZ	byte2	; inc next higher LSB
This is repeated for each DAW instruction.		

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: EUSART

The auto-baud measurement may not determine the correct baud rate if the ABDEN bit is set while the RB4/RX pin is low.

Work around

If the wake-up function is being used (WUE is set), wait for the RB4/RX pin to go high following a Break signal before setting the ABDEN bit.

If the wake-up function is not being used, ensure that RB4/RX is Idle (high between bytes) before setting the ABDEN bit.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first GOTO instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatably fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a NOP instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Oscillator (INTOSC)

The Least Significant bit of the OSCTUNE register, TUN0 (OSCTUNE<0>), is not implemented. As a result, incrementing or decrementing the OSCTUNE register will not have the expected single-step change on the frequency of INTOSC.

This is expected to be a permanent design change for the device.

Work around

For incremental changes to OSCTUNE, copy its contents to WREG, increment or decrement WREG twice, then write WREG back to OSCTUNE. This has the effect of incrementing or decrementing TUN5:TUN1 while maintaining TUN0 clear (the smallest possible adjustment in this silicon revision).

It is also possible to decrement OSCTUNE directly. Each direct decrement decreases the value of OSCTUNE by two (TUN0 remains clear). If incremental change is not required, OSCTUNE can also be written to directly with any value.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Oscillator (INTRC)

The 31 kHz internal RC oscillator source (INTRC) has been configured as a separate, fixed frequency source that is calibrated at the factory. Its output is no longer tunable using the OSCTUNE register. The INTOSC source remains tunable using OSCTUNE, as previously described.

This is expected to be a permanent design change for the device.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet

In the PIC18F1220/1320 Device Data Sheet (DS39605C), the following clarifications and corrections should be noted:

1. Module: Timer3 (Special Event Trigger)

In **Section 14.0 “Timer3 Module”**, bit 6 of the T3CON register was incorrectly defined as unimplemented. The correct definition for T3CON<6> is T3CCP2 and is shown in **bold** below:

In all tables and references to the T3CON register throughout the document, T3CON<6> should always be interpreted as the control bit, T3CCP2, and not as an unimplemented bit position.

REGISTER 14-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON
bit 7							bit 0

bit 6,3 **T3CCP2:T3CCP1:** Timer3 and Timer1 to CCP1 Enable bits
 1x = Timer3 is the clock source for compare/capture CCP module
 01 = **Reserved**
 00 = Timer1 is the clock source for compare/capture CCP module

2. Module: Data EEPROM

In Table 22-1 on page 254 of the Device Data Sheet, the typical value for parameter D122, Data EEPROM Erase/Write Cycle Time (TDEW) has changed. The new value is 5.5 ms and is shown in **bold** below.

TABLE 22-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D122	TDEW	Erase/Write Cycle Time	—	5.5	—	ms	

PIC18F1220/1320

REVISION HISTORY

Rev A Document (08/2005)

First revision of this document. Includes silicon issues 1 (Core), 2 (EUSART), 3 (Reset) and 4 (Oscillator (INTOSC Source)), and Data Sheet Clarification issues 1 (Timer3 (Special Event Trigger)) and 2 (Data EEPROM).

Rev B Document (03/2006)

Removed previous silicon issue 4 and added new silicon issues 4 (Oscillator/INTOSC) and 5 (Oscillator/INTRC). Data Sheet Clarification issue 1 (CCP) clarified as Timer3/Special Event Trigger.

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